



TAMPERE UNIVERSITY OF TECHNOLOGY

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**DESIGN OF A 2.4 GHZ ISM BAND POWER DIVIDER WITH
HIGHLY LINEAR SMALL-SIGNAL RF AMPLIFIER**

Master of Science Thesis

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Adj. Prof. Riku Mäkinen

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ABSTRACT

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This thesis report presents the design of a 2.4 GHz ISM band power divider with highly linear small-signal RF amplifier. The RF amplifier is used for compensating power loss caused as a result of a division operation. The prototyped power divider is used for the re-design of small-signal board that is utilized in the solid state cooking project with which required RF input signal is generated and supplied to the high power amplifier. With the re-designed small-signal board it is possible to configure the system as a single channel system or multichannel master/slave system. The prototyped power divider has two inputs (LO input and auxiliary input) and three outputs (Out 1, Out 2, and auxiliary output) with an unequal gain between the input and output ports. Although multiple power dividers are available in the market, we aimed to design a low cost power divider by making use of inexpensive components providing high performance. The prototyped power divider has the possibility for the mass production.

The objective of the thesis is to fabricate 3-and 2-way power dividers and highly linear small-signal RF amplifiers as standalone devices and then to realize the final power divider by integration of the dividers and amplifiers. The resistive power divider topology was chosen for the 3-and 2-way power dividers fabrication because of its advantages like, easy to implement, compact, and inexpensive. The specified gain design procedure was followed in the design of the RF amplifiers.

The prototyped 3-and 2-way power dividers have insertion loss of 9.88 dB and 6.26 dB respectively and minimum return loss of 21.7 dB is available in the operating frequency band, 2.4 - 2.5 GHz. The fabricated amplifiers are unconditionally stable up to 18 GHz. The input and output return loss of 17 dB and 10 dB gain amplifiers are 12.5 dB, 21.5 dB and 12.5 dB, 30.5 dB respectively with the power consumption of 66 mW. The gains are 17.2 dB and 11.2 dB, OIP3 of 29 dBm and 18 dBm respectively. The prototyped power divider has maximum gain between the inputs and Out 1 is 0.4 dB, Out 2 and auxiliary output is 1.24 dB. The return loss at all the input and output ports are above 19 dB. The price of all components is 3.5 euro. The prototyped power divider is good enough for the application.

PREFACE

This thesis report elaborates the work process of my final step towards getting a master's degree in Electrical Engineering from Tampere University of Technology, Finland. This thesis work has been carried out in RF Power and Base Stations department at NXP Semiconductors, Nijmegen, Netherlands as a part of the Solid State Cooking project from February 2013 - July 2013. This work has been supervised by Klaus Werner and Robin Stenfert. I would like to thank Dr. Klaus Werner, Program Manager, for giving me an opportunity to work on my thesis and for his continuous guidance, attention, comments, and mentorship from the beginning to the end

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADS	Advanced Design System
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CB	Common Base
CC	Common Collector
CE	Common Emitter
CPWG	Coplanar Waveguide with Lower Ground Plane
DC	Direct Current
FET	Field Effect Transistor
HB	Harmonic Balance
IIP3	Input Third-Order Intercept Point
IMD	Inter Modulation Distortion
IP3	Third-Order Intercept Point
ISM	Industrial Scientific Medical
ITU-R	International Telecommunication Radio Sector
LO	Local Oscillator
MAG	Maximum Available Gain
MCURVE	Microstrip Curved Bend
MLIN	Micro-strip Line
MSG	Maximum Stable Gain
MTEE	Microstrip Tee Component
MW	Micro Wave
MWI	Micro Wave Impedance
NXP	Next eXPerience
OIP3	Output Third-Order Intercept Point
PCB	Printed Circuit Board
RF	Radio Frequency
RL	Return Loss
SMA	SubMiniature version A connector
SSB	Small-Signal Board
SSC	Solid State Cooking
TOIP	Third-Order Intercept Point
VNA	Vector Network Analyzer
VSG	Vector Signal Generator
WLAN	Wireless Local Area Network
WSN	Wireless Sensor Networks

LIST OF SYMBOLS

dB	Decibel
dBm	Decibel milliwatts
E_g	generator voltage
G_A	available power gain
G_P	power gain
G_T	transducer power gain
h_{FE}	DC current gain
mm	milli meter
mA	milli ampere
nH	nano henry
pF	pico farad
P_{avg}	available power from the generator
P_{avn}	available power from the network
P_{in}	input power to the network
P_L	power delivered to the load
$P_{o(-1dB)}$	output 1-dB compression point
$P_{i(-1dB)}$	input 1-dB compression point
r_L	radius of load stability circle
r_s	radius of source stability circle
S_{11}	reflection coefficient at the input port
S_{12}	transmission coefficient from the output port to input port
S_{21}	transmission coefficient from the input port to output port
S_{22}	reflection coefficient at the output port
V	voltage
V^+	incident wave voltage
V^-	reflected wave voltage
V_{CC}	collector common voltage
W	watt
Z_0	characteristic impedance
ε_r	relative permittivity
Γ_s	source reflection coefficient
Γ_L	load reflection coefficient
Γ_{in}	input reflection coefficient
Γ_{out}	output reflection coefficient
Ω	Ohm
μ	load stability factor
μ'	source stability factor

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1. INTRODUCTION

Currently most of the engineering companies, for example, NXP Semiconductors, Freescale Semiconductors, Infineon, are paying extra attention in developing new devices or systems which are compatible with the industrial, scientific, and medical (ISM) frequency band. This is due to fact that, the ISM band is an unlicensed frequency band. Thus, it offers an attractive alternative over the high cost licensed frequency spectrum. Today the most popular license free ISM band is 2.4 GHz band and is available in many regions of the world. As a consequence the applications at this frequency band are growing rapidly. The ISM 2.4 GHz frequency band approximately ranges from 2.4 GHz to 2.5 GHz. In the electromagnetic frequency spectrum the ISM frequency part is defined by the International Telecommunication Radio Sector (ITU-R) on May, 1985. In addition to the microwave oven which operates at 2.4 - 2.5 GHz frequency band approximately centered at 2.45 GHz, the other communication devices those operating in this ISM band includes Wireless Local Area Networks (WLANs) and Wireless Sensor Networks (WSNs), Bluetooth, cordless phones, toys [1], [2], [3].

In the past the radio frequency (RF) energy (electromagnetic wave) was extensively used for radio communication. In recent years, there has been a lot of innovative research in RF energy which has brought tremendous advancements in the application areas. The examples include, RF plasma lighting, automotive (RF spark plugs), industrial, medical [4], [5]. One such exciting RF energy application and inspiration for this thesis work is the Solid State Cooking (SSC) technology. In this technology the conventional magnetron tube in the microwave oven used for generating the microwave radiation is replaced with the high power solid state amplifiers. The operating frequency of the magnetron tube in most of the countries is 2.4 GHz ISM band.

The conventional microwave oven uses the magnetron tube for generating microwave signals to cook/heat the food. These ovens are not capable of uniform distribution of RF energy within the cavity. One reason for this is due to the fact that the electromagnetic waves are not fully absorbed by the load (food) inside the cavity, this is because of the properties of the load. The absorption of the electromagnetic waves depends on many factors for instance, quantity, placement, and properties. The current microwave oven technology does not take into account the

fact that the absorption of the RF energy depends on the load properties. The second reason is the reflection of the electromagnetic waves inside the cavity. When the reflected signals are combined with the incoming the electromagnetic signals, then these signals have the property to either add or subtract with each other. This results in either a very high or very low power at random places within the cavity. This causes standing waves, which produces a non-uniform field inside the cavity. The current solution for this problem is the rotating plate. This exposes the load to the maximums and minimums simultaneously also it protects the load from overheating [6].

The SSC technology takes into account the properties of the load and also it takes advantages of these features. The properties of standing waves depend on several factors. The three important factors of the incoming waves are amplitude, frequency, and phase. By having more than one RF energy source (high power amplifier) and by varying their amplitudes, frequencies, and phases different wave patterns can be generated within the cavity. With this solution the load absorbs the RF energy from all sides. These high power amplifiers are required to be provided with an RF input signal at a required frequency and at a low power level for the purpose of driving the high power amplifiers. This is because the high power amplifiers can only amplify the RF input signal to a certain level. They are not capable of generating the RF input signal on their own. This signal generation at low power with a specific frequency is done by the Small-Signal Board (SSB). Figure 1.1 shows the block diagram of the system.

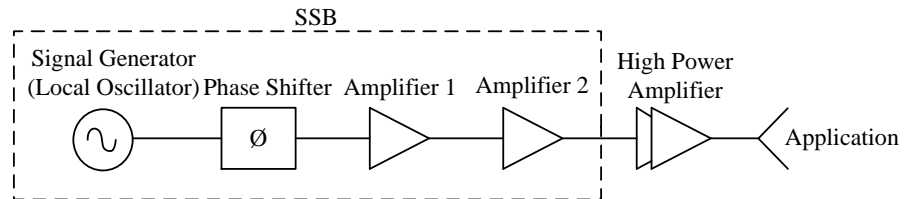


Figure 1.1. SSB and high power amplifier setup description.

The signal generator is a local oscillator which generates the RF input signal with a specific frequency. Then the signal goes through a phase change by the phase shifter. The signal is then amplified by a couple of amplifier stages before finally it is fed to the high power amplifier.

My role in this SSC project is to re-design the existing SSB. The re-designed SSB should have the flexibility to configure either in single channel or multi channel master/slave configuration and simultaneously to achieve modularity. With this re-designed SSB the application areas can be extended. In multichannel configuration the SSB should have the possibility of using the RF input signal generated by on-board local oscillator or RF input signal generated by the local oscillator on the other

channel. In master configuration, the RF input signal generated by the on-board local oscillator is distributed to the succeeding channels. On the other hand, in slave configuration, the SSB gets the RF input signal from the preceding master/slave channel; the on-board local oscillator is disabled with the software program in this configuration. The re-designed SSB should also provide the local oscillator signal as a reference signal for the control/monitoring purpose. This can be accomplished with a power divider. The power divider should have two inputs and three outputs. This thesis work presents the prototyping of this 2.4 GHz ISM band power divider. The signal power loss during the division operation is made up with the small-signal RF amplifier. The power divider is realized by 3-and 2-way power dividers and two small-signal RF amplifiers. Both, power dividers and amplifiers are designed and developed as a standalone device and the prototyping of the ISM band power divider is done by integration of all the fabricated devices on a single substrate.

1.1 Motivation

The aim of this thesis work is to prototype a low cost power divider which has two inputs and three outputs which operate at ISM 2.4 GHz band. Numerous power dividers are available in the market today but, less expensive, high performance, reproducibility, and compact solution is the main motive. Furthermore, the prototyped power divider is required to have the possibility of mass production with minimum deviation in the performance parameters in the operating frequency band. The small-signal amplifiers has to be developed by the use of NXPs active devices only. The more detailed design requirements are mentioned in Chapter 3.

1.2 Objectives and Scope of the Thesis

The objective behind this thesis work is to design and construct 3-and 2-way power dividers and amplifiers as a standalone devices and prototyping of ISM band power divider by integration of dividers and amplifiers. The scope of this thesis work is as follows:

- Literature review of the power dividers and small-signal RF amplifiers.
- Selection of suitable topology for the power divider realization.
- Selection of suitable small-signal RF amplifier design procedure.
- Designing and simulations in Agilent Advanced Design System (ADS).
- Fabrication and prototyping of both (dividers and amplifiers) devices as a standalone devices and performance measurements.
- Prototyping of ISM 2.4 GHz power divider by integration of dividers and amplifiers on a single substrate.

1.3 Thesis Outline

The whole thesis work is divided into 7 chapters. Chapter 1 is “Introduction” itself. Besides the introduction, it also covers thesis objectives and outline.

Chapter 2 is “Basics of Related RF Concepts”. It provides the basics related to elementary radio frequency design and performance parameters. These parameters are proving important in RF design and characterization. The performance parameters of a two-port network such as scattering (S)-parameters and stability factors are briefed. The impedance matching network design and selection of the DC bias circuits are also described. Additionally, the power gain relations and gain circles are also presented. Furthermore, linearity concepts are discussed at the end of this chapter.

Chapter 3 is “Theoretical Background and Design Goals”. It elaborates the literature review of different power divider topologies and amplifier design procedures. The different power divider topologies are discussed along with their implementation, advantages, and disadvantages. Finally, the specifications of the 3-and 2-way power dividers are tabulated. Then it follows the RF amplifier design procedures from different authors. Next, it follows the specified gain amplifier design procedure. Finally, the design requirements of the amplifiers which are used in realizing the power divider along with its purpose are detailed.

Chapter 4 is “Implementation” all about the implementation of the power dividers and small-signal RF amplifiers. First, the 3-way power divider design process is presented along with the simulation results, fabrication, and measurement results. A photograph of the fabricated 3-way power divider is also presented. Next, the 2-way power divider design flow is discussed in detail. Commercially available dividers on the market are also presented. Next, the detailed design description of the small-signal RF amplifiers is described. It includes the selection of transistor and RF design process. Along with this simulation results, layout and fabrication, and measurement results are also presented.

Chapter 5 presents the “Prototyping” of the power divider by integration of 3-and 2-way power dividers and two small-signal RF amplifiers on a single PCB. The simulation results of the power divider are given along with the layout. A photograph of the prototyped power divider and its measurement results are presented.

Chapter 6 is “Discussion” about the simulations and measurement results. Both, 3-and 2-way power dividers and amplifiers are discussed separately. Then, the prototyped power divider results are discussed.

Finally, Chapter 7 is all about the “Conclusion” and also some recommendations for the future work are suggested.

2. BASICS OF RELATED RF CONCEPTS

This chapter outlines the basics of RF concepts which are proving important in RF amplifier design. First, the Scattering parameters are presented with respect to the two-port networks. The Scattering parameters are considered as important parameters in the amplifier design and characterization. After this the stability issues and gain relations in the two-port networks are explained. Next, impedance matching concepts and DC bias circuits will be discussed. Finally non-linearities in amplifiers are introduced in Section 2.6.

2.1 Scattering Parameters

Linear and non-linear networks are characterized by measuring the parameters at the input and output terminals so called ports, by ignoring the actual contents inside the network [7]. In this context the parameters are the voltages at nodes and currents in branches. By applying simple open- and short-circuit conditions at ports these parameters are measured practically. However, it is only possible at low-frequencies [8]. This technique is not feasible at high frequencies. This is because the voltages at nodes and currents in branches changes more rapidly at higher frequencies. Therefore the measurement of voltages at nodes and currents in branches at high frequencies are highly problematic. In addition, the magnitude of the inductance of the wire can be significantly high while implementing the short-circuit condition. Also, the open-circuit condition can lead to capacitive loading. Moreover, the open- and short-circuit conditions at high frequencies lead the active device (transistor) to oscillate. In many cases these oscillations destroy the active device [9].

In order to overcome these problems at microwave (MW) and radio frequencies a new set of parameters called Scattering parameters or simply S -parameters are introduced. With these parameters the networks are modeled in terms of incident, reflected, voltage or current waves [10]. S -parameters are specifically used for small-signal representation of the network [9]. And besides, these parameters are used in modeling of passive and active components. The S -parameters are extensively used in the microwave and radio frequency design and measurements. Furthermore, the other parameters like, impedance (Z)-, admittance (Y)-, hybrid (H)-, and $ABCD$ -parameters can be derived from the S -parameters, the derivations are given in [8].

The S -parameter technique is a simple and yet most powerful tool used in RF and microwave engineering stream. The advantages of S -parameters over the other parameters are convenient to measure, easy to understand, and to work with at high frequencies. Moreover, they are more accurately measured parameters at microwave frequencies. In addition, they provide in-depth understanding of a design or measurement [7], [11]. The matrix representation of these parameters is called S -matrix.

Let us consider an amplifier as a two-port network, an input port, and an output port, as depicted in Figure 2.1 and the S -parameters of this two-port network is expressed in the following form [12] as

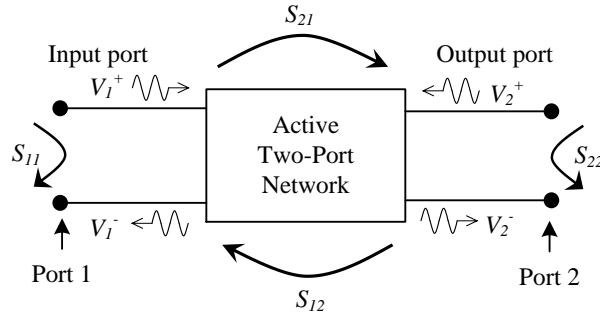


Figure 2.1. Two-port network S -parameters representation.

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+, \quad (2.1)$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+, \quad (2.2)$$

where V_1^+ , V_1^- are the incident wave and the reflected wave voltages at port 1, V_2^+ , V_2^- are the incident and reflected wave voltages at port 2, and S_{11} , S_{12} , S_{21} , and S_{22} are the S -parameters usually these are expressed in complex numbers. The S -matrix is described as

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}. \quad (2.3)$$

It is important to note that the DC power supply port of the amplifier is usually ignored in this type of modeling. Meaning that, the S -parameters of an amplifier are given for a particular bias current. Besides that, the S -parameters are expressed for a single frequency only. The matrix representation of equations (2.1) and (2.2) are as follows

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}. \quad (2.4)$$

Now, let us determine the S -parameters from equations (2.1) and (2.2). From equation (2.1) the S_{11} -parameter, the so called input reflection coefficient at port 1

is given by

$$S_{11} = \left. \frac{V_1^-}{V_1^+} \right|_{V_2^+=0}. \quad (2.5)$$

The condition $V_2^+=0$ in equation (2.5) means the wave entering at port 2 is zero. In other words, the port 2 is terminated with a matched load; in this case it is 50Ω . Commonly, the majority of the radio frequency and microwave systems are designed for 50Ω impedance. From equation (2.2) the S_{21} -parameter so called transmission parameter or forward gain or simply the gain from port 1 to port 2 is given by

$$S_{21} = \left. \frac{V_2^-}{V_1^+} \right|_{V_2^+=0}. \quad (2.6)$$

Next, the S_{22} -parameter, the so called output reflection coefficient from the equation (2.2) is given by

$$S_{22} = \left. \frac{V_2^-}{V_2^+} \right|_{V_1^+=0}. \quad (2.7)$$

The condition $V_1^+=0$ in equation (2.7) means the wave entering at port 1 is zero. Likewise, the S_{12} -parameter, the so called reverse isolation or reverse gain from port 2 to port 1 from (2.1) is given by

$$S_{12} = \left. \frac{V_1^-}{V_2^+} \right|_{V_1^+=0}. \quad (2.8)$$

In amplifiers, the S_{21} -parameter is usually expressed in decibels (dB), in logarithmic scale, commonly it is termed as gain. The Return Loss (RL) is a measure of how close the input and output impedances of an amplifier to the reference impedance, in most cases 50Ω . The input return loss of an amplifier is expressed as

$$RL_{IN(dB)} = 20 * \log_{10} \left| \frac{1}{S_{11}} \right|, \quad (2.9)$$

similarly, the output return loss as

$$RL_{OUT(dB)} = 20 * \log_{10} \left| \frac{1}{S_{22}} \right|. \quad (2.10)$$

Return loss is defined as the ratio of the reflected wave voltage to the incident wave voltage expressed in dB. S -parameters are utilized in further sections while dealing with the stability, power gains, and impedance matching networks.

2.2 Stability

Stability is an important parameter in the RF and MW amplifier circuit design. A typical amplifier will not oscillate with any passive load or source terminations. Stability is defined as the tendency of the amplifier to not oscillate. In the majority of the applications the stable performance of the amplifier is necessary. Since, if the amplifier oscillates it consumes more current by changing the bias condition results in an increase in power dissipation in the form of heat. Eventually it will damage the active device in the circuit [13]. Furthermore, the amplitude of the oscillations increases with time. When this signal level crosses the threshold level then the active device forced into large signal operation. This can also cause damage to it or any other connected device.

The presence of the feedback path in the circuits is one of the main reasons for the oscillations. The feedback can be of two types: positive feedback and negative feedback. In a positive feedback system, the magnitude of the reflected signal amplitude level is higher than the forward signal amplitude level. This increase in amplitude destroys the device by increasing the heat dissipation in the device itself. But, in a negative feedback system the reflected signal amplitude is lower than the forward signal amplitude level. The reflected signal will die out with the time. An amplifier may have the tendency to oscillate at any frequency ranging from the lower to higher frequencies. In the majority of the applications the stable operation of the amplifier at all frequencies is preferred. In other words, in most applications stable operation at the stop band frequencies is also important apart from the pass band frequencies. This is because, the oscillations in the stop band frequencies may mix up with the pass band frequencies and falls near to the pass band results in oscillations in the frequency of interest.

Other reasons for oscillations in amplifiers are due to fluctuations in temperature, bias currents, input signal level, the amplification of the device greater than unity, external circuits connected to it and its parasitic, or device internal feedback. In most cases, the last one is the main cause for any unwanted oscillations [14].

The stability of a two-port network can be described in two ways, unconditionally stable or potentially unstable. If the two-port network is unconditionally stable then it will not oscillate with any passive load or source terminations at all frequencies. The potentially unstable two-port network is stable only for certain frequencies and may have the tendency to oscillate for certain load or source terminations. In many cases, the main goal of the designer is to achieve the unconditional stability. It may be problematic for the designer to select the active device that is unconditionally stable at all frequencies. Nevertheless, the unconditional stability can be achieved by utilizing the stabilization techniques discussed in the following sections [15].

2.2.1 General Concept

Let us consider a two-port network that is connected to a generator at the one end and termination at the other end as shown in Figure 2.2, along with the reflection coefficients at the input and output ports.

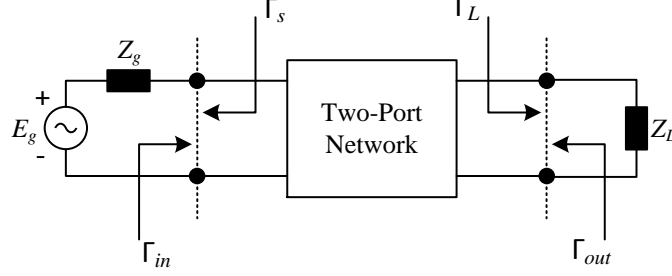


Figure 2.2. Two-port network reflection coefficients representation at every port along with source and load terminations.

Where Γ_L and Γ_s are the load and source reflection coefficients, Γ_{in} and Γ_{out} are the input and output reflection coefficients, E_g and Z_g are the generator and its impedance, and Z_L is the load impedance with which the two-port network is terminated.

If the absolute values of the input and output reflection coefficients are less than one [15] then the two-port network is unconditionally stable. Meaning that, if $|\Gamma_{in}| < 1$, then the amplitude of the reflected wave amplitude decreases (negative feedback) eventually die out with the time. On the other hand, if $|\Gamma_{in}| > 1$, then the amplitude of the reflected wave amplitude increases (positive feedback), which causes the active device to oscillate. Therefore, the conditions for the unconditional stability are identified as follows [8]

for

$$\Gamma_s < 1, \quad (2.11)$$

and

$$\Gamma_L < 1, \quad (2.12)$$

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1, \quad (2.13)$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| < 1. \quad (2.14)$$

From the equations (2.13) and (2.14) it can be observed that the two-port network stability is dependent on Γ_L , Γ_s , and S -parameters. Since the S -parameters are defined for single frequency from Section 2.1), the parameters on which the stability of the two-port network depends on are Γ_L and Γ_s . Depending on the values of the reflection coefficients (load and source) the stability of the two-port network can

be unconditionally stable or potentially unstable and is determined by the stability factors as follows.

2.2.2 Stability Factors

The stability of the two-port network is determined by the following stability factors: μ (Mu), μ' (Mu-prime), and Rollett stability factor k [15]. These are calculated with the S -parameters. According to the Rollett stability criterion the two-port network is unconditionally stable, if both

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1, \quad (2.15)$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} < 1, \quad (2.16)$$

are satisfied. In [14], [16] it is stated that, the other conditions which are used to determine the stability are almost similar to the stability factors mentioned in equations (2.15) and (2.16). The complete derivation of Rollett condition, $k > 1$, is given in [15].

The μ and μ' factors, the so called load stability factor and source stability factor respectively are also used to determine the stability of the two-port network in terms of the S -parameters. The conditions that are to be satisfied for unconditional stability of the two-port network referred to μ is given by

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*(S_{11}S_{22} - S_{12}S_{21})| + |S_{21}S_{12}|} > 1, \quad (2.17)$$

and, regard to μ' is given by

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*(S_{11}S_{22} - S_{12}S_{21})| + |S_{21}S_{12}|} > 1. \quad (2.18)$$

Either of μ or μ' is enough to determine the stability of a two-port network. Meaning that, a two-port network is unconditionally stable if $\mu > 1$ or $\mu' > 1$ [17]. If μ and μ' are less than or equal to one ($\mu \leq 1$ and $\mu' \leq 1$) then the two-port network is potentially unstable.

2.2.3 Stability Circles

As mentioned in Section 2.2, if the two-port network is potentially unstable ($\mu \leq 1$, $\mu' \leq 1$, $|\Gamma_L| > 1$, $|\Gamma_s| > 1$) then it may oscillate for certain combinations of load and source impedances. These impedances are determined with the help of the stability

circles by plotting on the Smith chart. The stability circle is the border line between the source or load impedances for which they cause the two-port network to oscillate and for which they do not [18].

From the equations (2.13) and (2.14) it can be observed that, Γ_{in} and Γ_{out} are dependent on the load and source terminations that is, Γ_L and Γ_s . First, let us consider Γ_{in} . For certain load impedances Γ_L can be greater than or less than unity. Since, for unconditional stability at the source side, the chosen load impedances should satisfy both $\Gamma_{in} < 1$ and also $\Gamma_L < 1$ simultaneously. In the same way, $\Gamma_{out} < 1$ and also $\Gamma_s < 1$ for unconditional stability at the load side. The borderline between the stable and unstable region at the load side can be interpreted by a circle called “the output stability circle” (Figure 2.3 (a)) for all values of Γ_L when $|\Gamma_{in}|=1$. The center, C_L , of the output stability circle is at

$$C_L = \frac{(S_{22} - (S_{11}S_{22} - S_{12}S_{21})S_{11}^*)^*}{|S_{22}|^2 - |(S_{11}S_{22} - S_{12}S_{21})|^2}, \quad (2.19)$$

and the radius, r_L , of

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |(S_{11}S_{22} - S_{12}S_{21})|^2} \right|. \quad (2.20)$$

Similarly, at the input side “the input stability circle” (Figure 2.3 (b)) is used to differentiate the stable and unstable regions. The input stability circle is plotted for Γ_s when $|\Gamma_{out}|=1$. The expressions for the center, C_S , and radius, r_S , of the input stability circle are given in [15].

Furthermore, $\mu > 1$ and $\mu' > 1$ gives the minimum distance between the center of the Smith chart and the unstable regions in Γ_L and Γ_s plane.

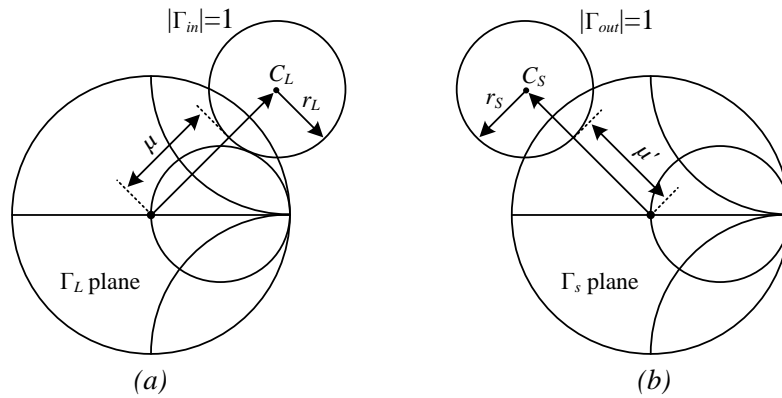


Figure 2.3. Stability circles of a two-port network plotted on the Smith chart: (a) Output stability circle on the Γ_L plane center is at, C_L , is a complex number. With a radius of r_L , where μ is the minimum distance between the center of the Smith chart and the unstable region, (b) Input stability circle on the Γ_s plane center is at, C_S , is a complex number. With a radius of r_S , where μ' is the minimum distance between the center of the Smith chart and the unstable region.

By considering the absolute values of the S_{11} , S_{22} , Γ_{in} , and Γ_{out} the stable and unstable regions on the Smith chart can be predicted with respect to the stability circles. If $\Gamma_L=0$, $\Gamma_s=0$ and if $|S_{11}|<1$, $|S_{22}|<1$ then, $|\Gamma_{in}|<1$ and $|\Gamma_{out}|<1$ is true therefore, the two-port network is stable. In this case, if the input and output stability circles include the center of the Smith chart then the stable region is inside the stability circle. If the center of the Smith is excluded then the outer region of the stability circle is the stable region (Figure 2.4 (a) and (c)). Likewise, if $|S_{11}|>1$, $|S_{22}|>1$ then, $|\Gamma_{in}|>1$ and $|\Gamma_{out}|>1$ is true therefore, the two-port network is unstable. In this case, the region inside the stability circle is the unstable region if it encloses the center of the Smith chart. If the stability circle excludes the center of the Smith chart then the outer region of the stability circle is the unstable region (Figure 2.4 (b) and (d)) [15].

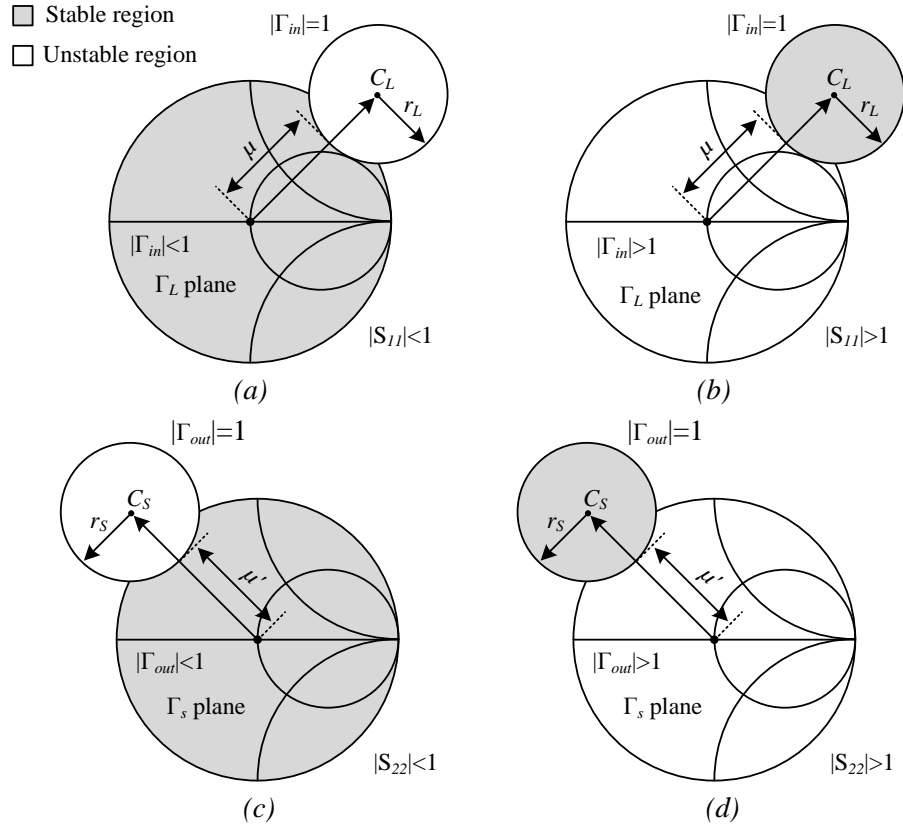


Figure 2.4. Representation of the stable and unstable regions on the Smith chart with respect to the stability circles: (a) Output stability circle with stable region outside the stability circle on Γ_L plane, (b) Output stability circle with stable region inside the circle on Γ_L plane, (c) Input stability circle with the stable region outside the stability circle on Γ_s plane, (d) Input stability circle with the stable region inside the circle on Γ_s plane.

A potentially unstable two-port network can be made unconditionally stable by employing stabilization techniques. They are, inductive degeneration technique, base and collector resistive (series or shunt) loading, or a feedback network. Usually the resistive loading is implemented either in series, in shunt, or both at the output

with the cost of the degradation of the circuit performance, mainly gain. More theoretical and mathematical information on stability is available in [13], [15], [17], and [19].

2.3 Power Gain Relations and Gain Circles

Let us consider a two-port network connected to a generator and to a load termination as shown in Figure 2.5. Four powers which can be identified at every port in that two-port network are: available power from the generator, P_{avg} , the input power to the two-port network, P_{in} , available power from the two-port network, P_{avn} , and power delivered to the load, P_L [20].

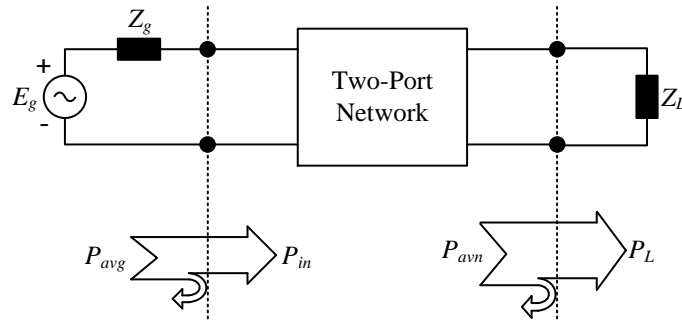


Figure 2.5. Representation of powers at every port in a two-port network.

The power gains such as, available power gain, G_A , transducer power gain, G_T , and power gain, G_P , are defined in terms of powers at every port and S -parameters as follows. The transducer power gain, G_T , is the actual gain of the two-port network including the input and output matching networks (discussed in Section 2.4). In terms of powers it is defined as the ratio of the power delivered to the load, P_L , to the available power from the generator, P_{avg} . This is expressed in the following form as [21]

$$G_T = \frac{P_L}{P_{avg}} = \frac{(1 - |\Gamma_L|^2)|S_{21}|^2(1 - |\Gamma_s|^2)}{|(1 - S_{22}\Gamma_L)(1 - S_{11}\Gamma_s) - S_{12}S_{21}\Gamma_L\Gamma_s|}. \quad (2.21)$$

G_T is dependent on both Z_g and Z_L , and both are equal to the characteristic impedance, Z_0 . The more simplified form of G_T is obtained by substituting in either of the equation (2.13) or equation (2.14) which also helps in deriving G_A and G_P . For instance, by making the load reflection coefficient (Γ_L) is equal to the complex conjugate of the output reflection coefficient (Γ_{out}^*), and by substituting it in equation (2.21) yields available power gain G_A . In powers, it is defined as the ratio of available power from the network, P_{avn} , to the available power from the generator, P_{avg} . The expression for G_A is given as

$$G_A = \frac{P_{avn}}{P_{avg}} = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|} |S_{21}|^2 \frac{1}{1 - |\Gamma_{out}|^2}, \quad (2.22)$$

G_A depends only on Z_g not on Z_L .

Next, power gain G_P is also known as operational power gain and is defined as the ratio between the input power, P_{in} , and power delivered to the load, P_L . It depends only on Z_L not on Z_g . The expression for G_P is given as [15]

$$G_P = \frac{P_{in}}{P_L} = \frac{1}{1 - |\Gamma_{in}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{1 - |S_{22}\Gamma_L|^2}. \quad (2.23)$$

With the help of G_A and G_P the gain circles are described. The gain circles are drawn on the Smith chart. In the amplifier design, these gain circles are used to locate the available gain and power gain. In addition to G_A , G_T , and G_P , the other gains such as, maximum available gain (MAG) and maximum stable gain (MSG) are also commonly described. The MAG and MSG are generally used in the data sheets to represent the maximum capabilities of the transistor [8]. The MAG is defined as the maximum transducer gain. That is, it is the maximum gain possible to achieve with the conjugate matching in a two-port network. The transistor should be unconditionally stable ($k > 1$) for calculating the MAG. The highest gain that is possible to achieve from a potentially unstable two-port network after making it stable is the MSG and is expressed in the following form:

$$MSG = \frac{|S_{21}|}{|S_{12}|}. \quad (2.24)$$

2.4 Impedance Matching Networks

In the high-frequency design, maximum transfer of power at every port is often an important requirement with less possibility of reflections and also with low signal energy loss. This can be accomplished by a network called “impedance matching network” which transforms the source impedance to the load impedance. A simple two-port network with the impedance matching networks at the input and output is shown in Figure 2.6. Generally, matching networks are deployed at the input and output of an amplifier.

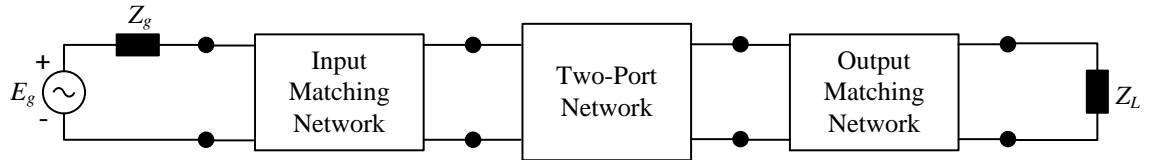


Figure 2.6. Two-port network with the input and output matching networks.

The input impedance matching network transforms the two-port network input impedance to the generator impedance, Z_g . Thus, the maximum input signal power

is fed into the two-port network. Similarly, with the output matching network maximum power is delivered to the load from the two-port network output. Additionally, it protects the two-port network from the reflections caused by the impedance mismatch resulting from the external circuits connected to it [18], [22].

The following attributes should be considered while designing the impedance matching network [23]:

- Complexity - It is always wise to choose a simple, with few possible components as an impedance matching network with which the design specifications can be accomplished. The impedance matching network with fewer components can be inexpensive, compact, and also will introduce less loss.
- Bandwidth - There are numerous topologies available to design a matching network for the single frequency only. However, in many applications, a band of frequencies needs to be matched to the load. In this situation, the complexity of the matching network increases and also it can be less reliable.
- Implementation - Based on the type of application, power level, frequency of operation, and PCB area available, the matching networks are designed. These matching networks can be composed of lumped components (resistors, inductors, or capacitors), quarter-wave transformers, and stubs. In some cases, their combinations are also preferred.
- Adjustability - In some applications, an adjustable matching network needs to be designed for various load impedances after the circuit is fabricated. In these situations, inductors or capacitors can be used. Because, it is easier to modify lumped components than stubs or quarter wave transformers, for that matter.

Impedance matching can be accomplished either with stub (single stub or double stub) or discrete components. The stub matching networks are more complex compared to the other circuits. The discrete component impedance matching networks are more often preferred at radio frequencies. These are made up of resistive elements, reactive elements or both. The first mentioned one is not practically used because it dissipates power and also introduces noise to the circuit. The reactive elements (inductor or capacitor) impedance matching networks are the simplest and most widely used matching networks. These are categorized into two types. The first type is a two element network, a so called L-network. The second type is a three-element network. Eight possible combinations of L-network matching networks are given in [8].

2.5 DC Bias Circuits

The main purpose of the DC bias circuit is to retain the DC operating point stable against the temperature fluctuations. The DC operating point is also known as DC bias point or simply quiescent (Q) point. For instance, in bipolar junction transistors (BJT) the DC current gain, h_{FE} , and the base-to-emitter voltage, V_{BE} , are the parameters which are dependent on the variations in the temperature. A raise in the temperature will result in decrease of a V_{BE} at a rate of $2.5 \text{ mV}/^{\circ}\text{C}$ and also increase of h_{FE} at a rate of $0.5\%/^{\circ}\text{C}$ from its theoretical value at room temperature [18]. Furthermore, h_{FE} is also dependent on the process variations. It is almost impossible to manufacture two identical devices with respect to h_{FE} . Most often this is the reason for wider specification of the DC current gain.

One solution to overcome these problems is by utilizing an active bias circuit. More often it employs an IC or an extra active device (generally transistor), and less resistors which keeps V_{BE} and I_C constant against variation in h_{FE} and temperature drifts. But, due to the cost considerations these circuits are generally not preferred. However, the active bias circuits are widely used in applications where higher temperature variations are expected. And also, in applications where cost is not a big concern.

Unlike active bias circuits, the passive bias circuits are the most popular and most widely preferred bias circuits even though these circuits offer stable DC bias point operation over a moderate temperature variations. This is because, the passive bias circuits are easy to implement and uses only a few resistors. Furthermore, these are easy to understand compared to the active bias circuits.

The simple non-stabilized BJT bias circuit which uses two resistors, base resistor, R_B , and collector resistor, R_C , along with two DC supply voltages, V_{BB} and V_{CC} is shown in Figure 2.7 [24]. The base current, I_B , which flows into the transistor is set by R_B . The collector current, I_C , is simply h_{FE} times I_B . The collector-to-emitter voltage, V_{CE} , is calculated by subtracting the collector voltage drop, V_C , across R_C , from the supply voltage, V_{CC} . If I_C varies, V_{CE} also varies depending on the voltage drop across R_C . The variation in I_C due to process is directly proportional to h_{FE} for a fixed V_{CC} and V_{BE} . Meaning that, for example, a 5% increase in h_{FE} will causes a 5% increase in I_C . Hence, the non-stabilized BJT bias circuits do not compensate the variations in h_{FE} . However, V_{BB} and V_{CC} bias conditions can be varied for compensating h_{FE} variations.

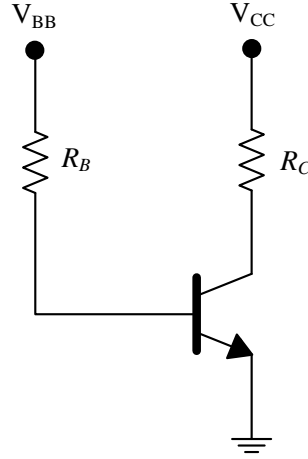


Figure 2.7. *Non-stabilized passive BJT bias circuit.*

The voltage feedback BJT bias circuit (Figure 2.8 (a)) decreases the variations in I_C , which occurs due to variations in h_{FE} . This is accomplished with the collector to base feedback resistor, R_B . The base current, I_B , is derived from V_{CE} which is opposed by V_{CC} . An increase in I_C due to variations in h_{FE} increases the voltage drop across R_C . This in turn decreases the collector-to-emitter voltage, V_{CE} , which causes the I_B to decrease, then I_C . In simple words, voltage feedback bias circuit reduces the quantity that the collector current increased due to h_{FE} . Meaning that, the base resistor forms the negative feedback. In addition, it is the most widely used inexpensive, simple DC bias circuit in radio frequencies. The emitter terminal is directly connected to the ground. Thus very low emitter lead inductance is possible. The voltage feedback with current source BJT bias circuit (Figure 2.8 (b)) is particularly used when V_{CC} and V_{CE} are greater than 15 V and 12 V. The bias circuit shown in Figure 2.8 (c) is often employed in power amplifiers. The emitter feed BJT bias circuit (Figure 2.8 (d)) is usually used at low frequencies. Because, at high frequencies the emitter resistor RE provides high AC gain loss [24].

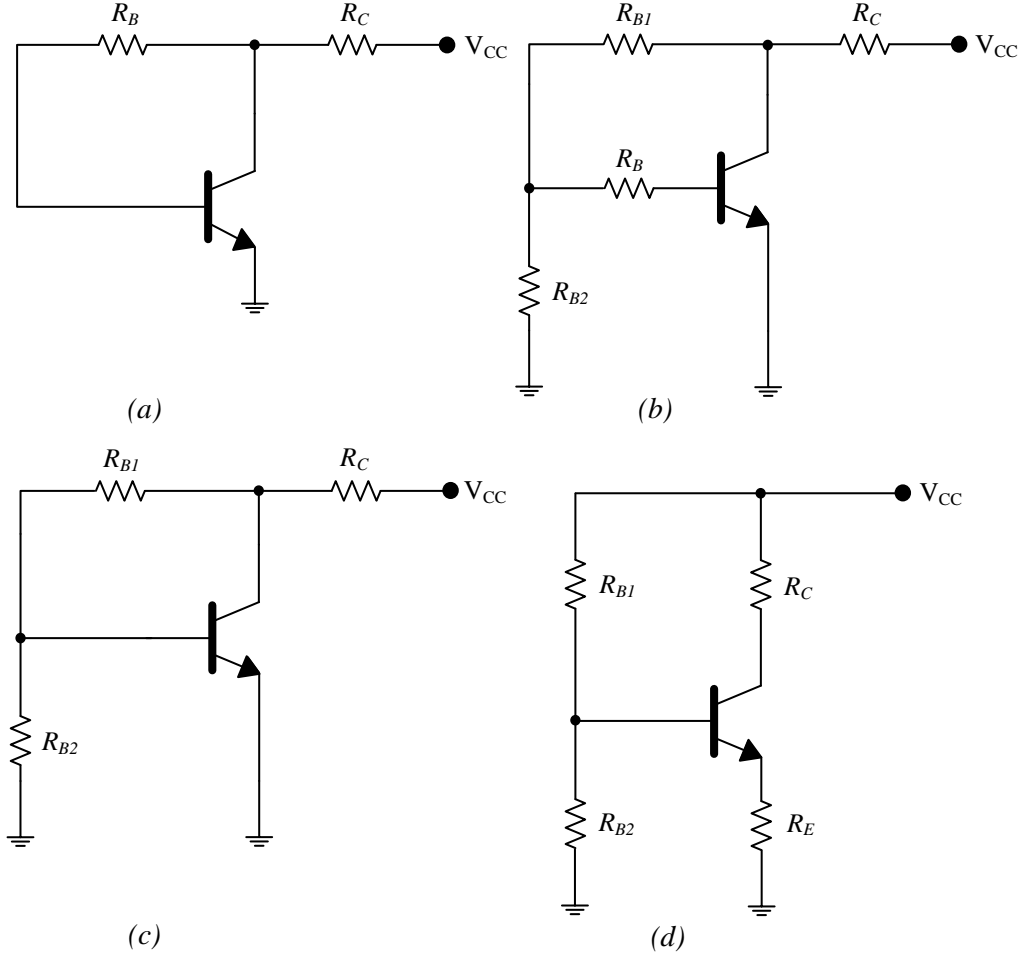


Figure 2.8. Passive BJT bias circuits [24]: (a) Voltage feedback, (b) Voltage feedback with a current source, (c) Voltage feedback with a voltage source, (d) Emitter feedback.

2.6 Non-linearities in Amplifiers

An amplifier whose output response is a non-linear function of the input signal is said to be a non-linear amplifier. If the amplitude of the input signal exceeds a certain limit then the output response may not be in linear relation to the input signal. Since, the amplifier is pushed into saturation. This results in different types of distortions are as follows [13], [25]:

- Frequency Distortion - is exhibited if the active components in an amplifier amplifies certain frequency amplitudes differently than the other frequencies. This type of distortion is more often observed in situations where the amplifier is pushed to operate at its extreme limits.
- Amplitude Distortion - is also known as non-linear distortion. If the amplifier is not properly biased then the transistor is pushed into either saturation or cut-off region. This results in amplitude distortion.
- Harmonic Distortion - by the application of the sinusoidal signal as an input

to a non-linear circuit, for instance amplifier, the output spectrum can have frequency components which are integer multiples of the input signal. This type of distortion is known as harmonic distortion.

- Gain Compression - means decreasing the gain of an amplifier with an increase in amplitude of the input signal. It is due to the operation of the transistor in saturation.
- Cross Modulation - this phenomenon occurs when a weak desired signal and a strong interfering signal passes through a non-linear (amplifier) circuit. The modulation is shifted from the strong interfering signal to the weak desired signal. Generally, this is noticed in amplifiers when the amplifier amplifies signals from different channels at the same time. For example, in television transmitters.
- Intermodulation Distortion - when the input signal consists of two or more interference signals which are closely spaced with respect to the main signal frequency then the non-linear system produces intermodulation components which interfere with the desired signal. In this situation, the output spectrum exhibit components that are not harmonics of the input signals. This is due to the mixing (multiplication) of the two frequencies.

In this work, our main focus is only on gain compression and intermodulation distortion.

2.6.1 The 1-dB Compression Point

The 1-dB compression point is used to represent the power level that an amplifier can handle. In other words it is the power level limit beyond which the amplifier deviates from its linear characteristics by 1 dB. There are two types of 1-dB compression points, first one, output 1-dB compression point, $P_{o(-1dB)}$, second one, input 1-dB compression point, $P_{i(-1dB)}$. The first mentioned one gives the maximum output power level that an amplifier can deliver at the 1 dB point. Likewise, the maximum input power level that an amplifier can still operates in linear region is represented by the second one [26]. The relation between the input and output powers with respect to the gain of an amplifier is shown in Figure 2.9. The thick line shows the actual gain characteristics of an amplifier whereas the long dashed line gives the ideal characteristics. The horizontal coordinate of the dotted line gives $P_{i(-1dB)}$ and below vertical dotted line gives $P_{o(-1dB)}$. Generally, it is specified either at the input or output of an amplifier. If we know the input or output 1-dB power level limit the other can be calculated with an expression given by

$$P_{o(-1dB)} = P_{i(-1dB)} + (Gain - 1). \quad (2.25)$$

The 1-dB compression point is expressed in dBm. For instance, if the specified $P_{o(-1dB)}$ of an amplifier is +5 dBm then it is capable of delivering at least +5 dBm [13].

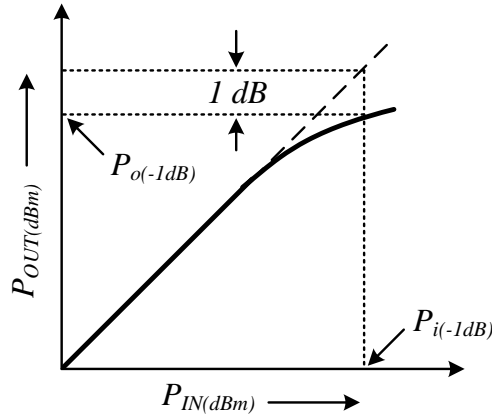


Figure 2.9. 1-dB compression point representation in amplifiers.

2.6.2 Third Order Intercept Point

The intermodulation distortion (IMD) products are generated if the harmonically created frequencies of the non-linear system are related to the input fundamental frequencies. The IMD products are produced as a result of mixing of interfere with the carrier, harmonics, IMD products from the preceding stages and from the other channels, or from the spurious responses created by the side bands. These IMD products may fall in in-band frequencies or cause out-of-band frequencies to fall in in-band frequencies. The intermodulation distortion is produced when operating frequencies are closely spaced from each other. Specially, in RF systems intermodulation distortion is problematic. For example, if the input signal frequencies f_1 and f_2 which are close to each other are applied to a non-linear system. Then the output spectrum will have numerous frequencies which are sum and difference of the fundamental frequencies, the so called second order products $f_1 + f_2$ and $f_2 + f_1$, and intermodulation products of $m f_1 \pm n f_2$, where $m+n$ gives the order of the distortion, and m and n are the whole numbers. The third-order ($m+n=3$) intermodulation products are problematic in RF system design. This is because, the third-order IMD products such as $2f_1 - f_2$, $2f_2 - f_1$, $3f_1$, and $3f_2$ out of which first two products are fall in the close vicinity of fundamental frequencies f_1 and f_2 as shown in Figure 2.10.

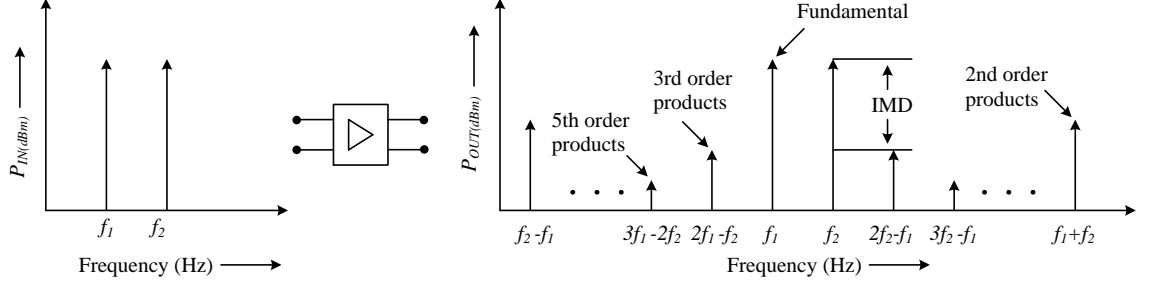


Figure 2.10. Representation of intermodulation products produced in amplifiers due to non-linearities [27].

Filtering out of $2f_1-f_2$ and $2f_2-f_1$ products are considerably difficult since they are very close to the pass band frequencies. The intermodulation distortion is the difference between the fundamental frequency power level and third-order intermodulation products power (Figure 2.10).

The intermodulation products in an amplifier are expressed in the figure of merit and is called third-order intercept point (TOIP or IP3). The IP3 is measured with a tow-tone test. In $2f_1-f_2$, $2f_2-f_1$, $3f_1$, and $3f_2$, the first two products are two-tone third-order intermodulation products. Since, they are generated by applying two-tones at the input simultaneously. The two-tone output third-order intercept point, OIP3, is calculated with the help of following expression

$$OIP3 = P_{out} + \frac{\Delta}{2}, \quad (2.26)$$

where, P_{out} is the output power of the each tone in dBm, P_{int} is the intermodulation power in dBm and $\Delta = P_{out} - P_{int}$ in dB as shown in Figure 2.11.

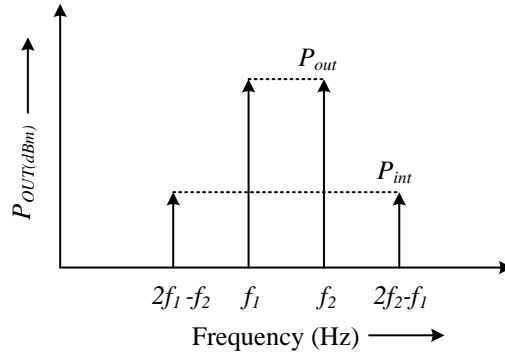


Figure 2.11. Third-order intermodulation products in amplifiers.

Furthermore, two-tone input third-order intercept point, IIP3, is calculated from the OIP3 and gain as

$$IIP3 = OIP3 - Gain, \quad (2.27)$$

The third-order intermodulation products power level increase/decrease by 3 dB for every 1 dB increase/decrease in input fundamental signal power [27]. Meaning,

with increase in input signal level the intermodulation products increases rapidly as shown in Figure 2.12. The thick line is the actual response of the amplifier and thick dashed line is third order intermodulation products. The intersection of these lines is the IP3. Additionally, the horizontal coordinate of IP3 is denoted as IIP3 and vertical coordinate as OIP3. OIP3 is more commonly used in amplifiers. More detailed information on non-linearity in amplifiers is reported in [13], [27], [28].

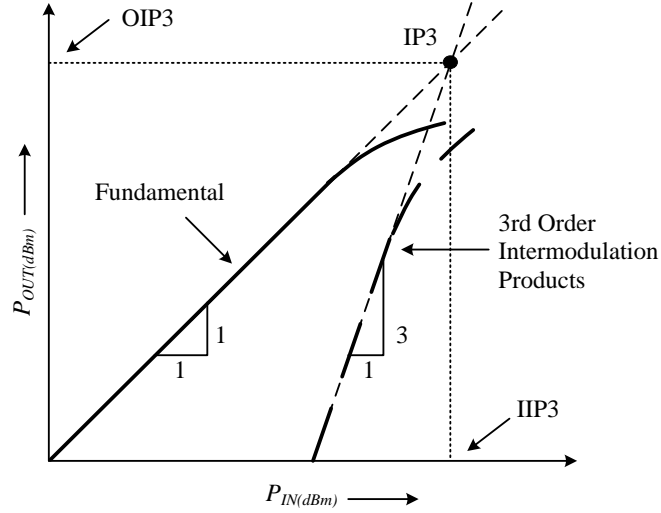


Figure 2.12. Representation of OIP3 and IIP3 in amplifiers.

3. THEORETICAL BACKGROUND AND DESIGN GOALS

This chapter is mainly divided into two sections. The first, section provides a brief overview of power dividers. The various types of resistive power dividers along with the schematics are presented. Then the design goals of the power dividers are listed.

The second section is all about the literature review of the RF amplifiers, possible amplifier configurations, and amplifier design procedures. It starts with the small-signal RF amplifiers introduction. Next, amplifier configurations then the design procedure of the RF amplifiers from five different authors are presented. Then the specified gain amplifier design procedure is also described. In Section 3.4 and 3.5 the design goals of the 17 dB and 10 dB gain small-signal RF amplifiers are listed respectively.

3.1 Power Dividers

In many radio frequency and microwave applications it is necessary to distribute the power among various paths simultaneously. And also in some applications it is necessary to provide the power to various lines from the same source. A simple possible way this can be accomplished is with a device called power divider/splitter. The resistor configuration used to separate the power is the basic difference between the power divider and power splitter [29]. Both, power dividers and power splitters, can be realized either with transformers, lumped elements, quarter wave transformers, micro-strip lines or strip lines.

A simple power divider which employs lumped component three-resistors and power splitter with two-resistors are shown in Figure 3.1 [30]. It is important to note that power dividers and power splitters are not interchangeable. Power dividers are symmetrical and bidirectional devices. Meaning that, apart from the power division power dividers can also be used in power combining applications. Like, in communication receivers where power from different sources are to be combined and also in power amplifiers to combine the power from different power amplifiers. The other applications of power dividers include, providing a sample signal for synchronization or for monitoring purpose, in test systems to measure the frequency, power and phase, for feedback, and in IMD measurements.

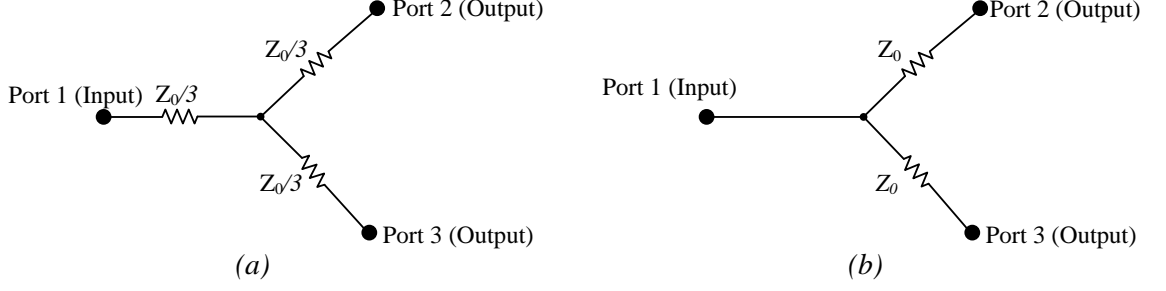


Figure 3.1. Power divider and power splitter [30]: (a) Three-resistor power divider, (b) Two-resistor power splitter.

The block diagram of a three-port network, one input port and two output ports, that is used as a power divider and a combiner is shown in Figure 3.2. As a power divider, it takes input power, P_1 , and provides two output powers, P_2 and P_3 , with an attenuation of α dB. The power combiner performs the opposite action as that of power divider. That is, it takes two powers as input powers, P_1 and P_2 and provides its sum, P_3 , ($P_3 = P_1 + P_2$) at the output port.

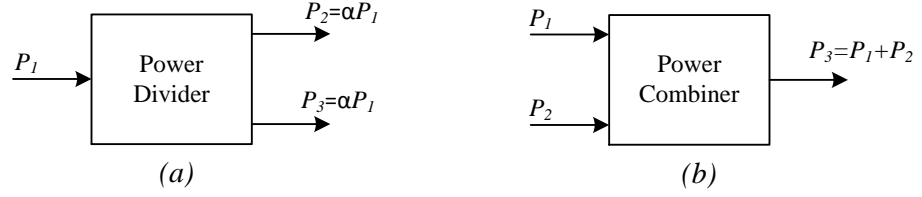


Figure 3.2. Power divider and power combiner [23]: (a) Power Divider, (b) Power Combiner.

The power dividers are either three-port, or four-port, or more port devices. And, also they can be either lossless or lossy. A basic three-port power divider provides equal split (3 dB) of power among the two output ports. It is also possible to have an unequal power divider. The typical specifications of the power divider that are to be achieved with the design based on the application are low insertion loss, good return loss, high isolation, higher bandwidth, and small size [9].

If we consider a basic T-junction transmission line (three-port) lossless power divider as shown in Figure 3.3 that has one input port and two output ports.

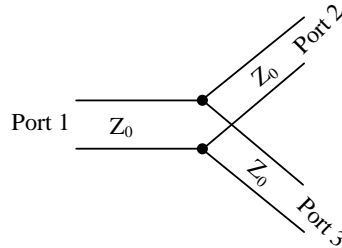


Figure 3.3. T-junction loss less power divider.

Then, the scattering matrix of this divider will have nine independent parameters is given by

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix}. \quad (3.1)$$

Ideally, if all the three-ports are matched to the standard characteristic impedance (Z_0) of 50Ω , then simplified form of the equation (3.1) is given as

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{21} & 0 & S_{23} \\ S_{31} & S_{32} & 0 \end{bmatrix}. \quad (3.2)$$

In order to maintain the equal power at three ports without any loss, it has to satisfy the following conditions

$$|S_{12}|^2 + |S_{13}|^2 = 1, \quad (3.3)$$

$$|S_{12}|^2 + |S_{23}|^2 = 1, \quad (3.4)$$

$$|S_{13}|^2 + |S_{23}|^2 = 1, \quad (3.5)$$

$$S_{13}^* S_{23} = 0, \quad (3.6)$$

$$S_{23}^* S_{13} = 0, \quad (3.7)$$

$$S_{12}^* S_{13} = 0, \quad (3.8)$$

From the above equations, it is apparent that the three-port network cannot be reciprocal, lossless, and matched at the same time. By compromising any parameter the real device can be realized. A passive device that is reciprocal and matched at all ports by compromising with the loss is a resistive power divider. Another passive device, with less loss, matched at all ports is reactive power divider. It is a non-reciprocal device [23].

3.1.1 Resistive Power Dividers

Let us consider a lossy three-port power divider that was built using the lumped components resistors by ignoring the isolation. Further, the three-ports are matched to the characteristic impedance as shown in Figure 3.4 [23]. It provides the equal split (3 dB) of the input signal between the output ports. It should be mentioned that, the unequal split divider can be also possible with resistive power divider.

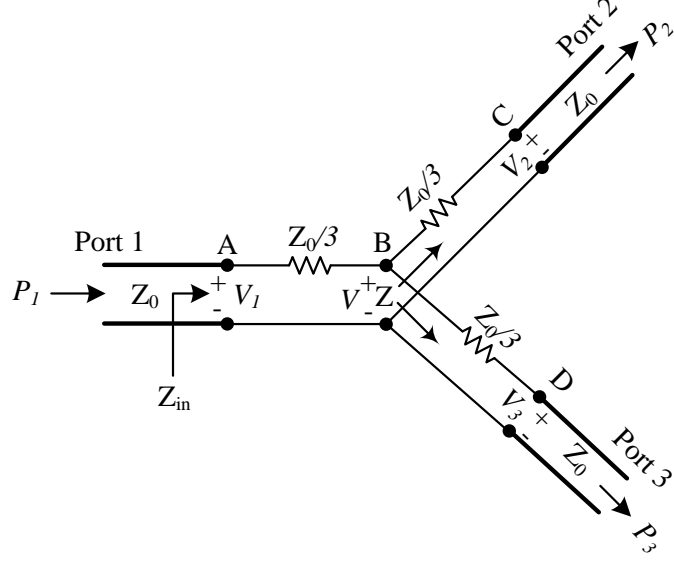


Figure 3.4. Three-port equal split resistive power divider [23].

If we assume that all the three ports are terminated with Z_0 , then the impedance, Z , seen by looking at P_2 and P_3 through $Z_0/3$ resistor is given by

$$Z = \left(\frac{Z_0}{3} \right) \parallel \left(\frac{Z_0}{3} + Z_0 = \frac{2Z_0}{3} \right). \quad (3.9)$$

Then, the input impedance, Z_{in} , seen at the input of the power divider is given by

$$Z_{in} = \frac{Z_0}{3} + Z. \quad (3.10)$$

By substituting equation (3.9) in equation (3.10) results in

$$Z_{in} = \frac{Z_0}{3} + \frac{2Z_0}{3} = Z_0. \quad (3.11)$$

Thus, the input port is matched to Z_0 . It is due to the reason that, all the three-ports are symmetrical and also matched. Means, $S_{11}=S_{22}=S_{33}=0$.

The voltage, V , at node B is given by

$$V = V_1 \times \frac{2Z_0/3}{Z_0/3 + 2Z_0/3} = \frac{2}{3}V_1. \quad (3.12)$$

Then, the voltages at nodes C and D are equal and is given by

$$V_2 = V_3 = V \times \frac{Z_0}{Z_0 + Z_0/3} = \frac{3}{4}V. \quad (3.13)$$

By substituting equation (3.12) in equation (3.13) results in the following expression

$$V_2 = V_3 = \frac{1}{2}V_1. \quad (3.14)$$

Thus, $S_{21}=S_{31}=S_{23} = -6$ dB, meaning that the output power level at port 2 and port 3 is 6 dB below the input power level at port 1.

Two possible topologies of the resistive power dividers are as follows [31], [32]:

- Delta resistive power divider - in this topology the resistors are arranged in a delta (Δ) fashion as shown in Figure 3.5 a three port equal-split delta resistive power divider. The drawback of this type of power dividers is that if the number of output ports increases then the complexity of the divider increases. Additionally, the calculation of resistor value becomes complex.

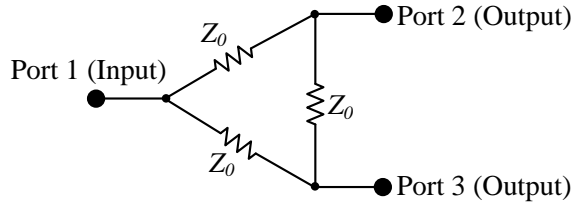


Figure 3.5. *Equal-split delta resistive power divider.*

- T-junction resistive power divider - the configuration of the resistors in this topology resembles the letter T. It is also called a Y resistive power divider. It is the most preferred topology for the resistive power dividers. Because of its advantages which includes, less complex, simple to understand, easier to calculate resistor values, and the resistor values are lower than that of delta topology (Figure 3.1 (a)).

The calculation of the resistor values in an arbitrary output port T-junction resistive power divider are as follows:

All the resistor values in the resistive power divider are same. The resistor value of an N-way T-junction resistive power divider is calculated with the help of the following formula

$$R = Z_0 \times \left(\frac{N-1}{N+1} \right), \quad (3.15)$$

where, Z_0 is the characteristic impedance, R is the resistor, and N is the number of output ports.

The insertion loss in dB is calculated with the formula as given below,

$$InsertionLoss = 10 * \log_{10}((1/N)^2)dB. \quad (3.16)$$

For instance, a four-port power divider is termed as 3-way (three output ports) power divider. It is a four-port device out of which one is the input port and the

remaining three ports are output ports.

3.1.2 Reactive Power Dividers

Reactive power dividers are the dividers those have isolation between the ports and all the port are matched simultaneously. An example of a reactive power divider is the Wilkinson power divider, which is realized with the micro-strip lines as shown in Figure 3.6.

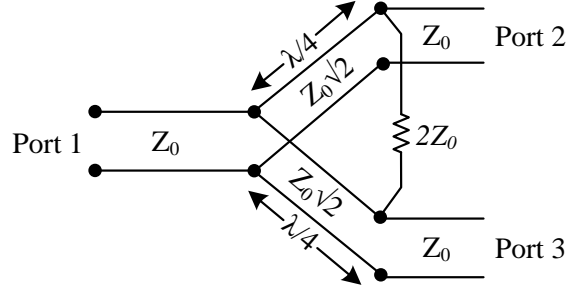


Figure 3.6. Three-port equal-split Wilkinson power divider [23].

In this work we will continue with the resistive power dividers only because of its advantages such as, they are compact, realized with lumped components, extremely broad band of operation, and are the only power dividers that can operate from DC onwards, and more importantly suitable for mass production. More detailed information on reactive power dividers can be found in [25] and [33]. A brief evaluation of power dividers is presented in [34].

3.2 3-and 2-way Power Dividers Design Goals

The 3-way power divider port 1 is connected to the output of the signal generator (local oscillator). The second port (port 2) is an auxiliary input. Port 3 is an auxiliary output and port 4 is directly connected to the phase shifter input (Figure 3.7). When the system is configured as a single channel system the auxiliary input and auxiliary output are terminated and the RF input signal from the local oscillator is selected as source for the phase shifter. In a multi channel master configuration the auxiliary input is terminated and the RF input signal is divided over the phase shifter and the auxiliary output port.

In multichannel slave configuration, the on-board local oscillator is turned off and acts as a $50\ \Omega$ termination. The RF input signal from the auxiliary input (connected to the auxiliary output of the previous channel which provides the RF input signal) will be divided among the phase shifter and auxiliary output. In a multi channel configuration the auxiliary input will be connected to the auxiliary output of either the master or the preceding slave small-signal board in a daisy chain system.

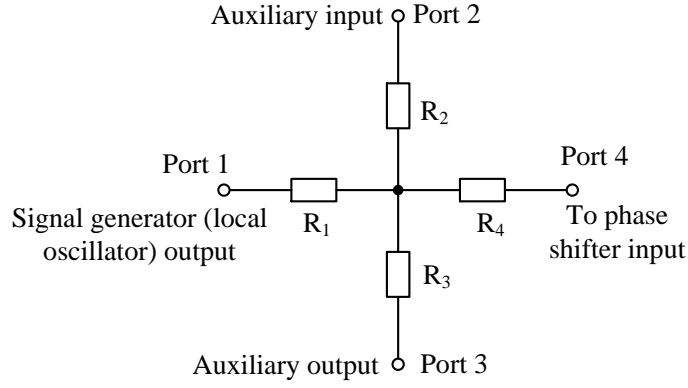


Figure 3.7. 3-way power divider showing the input and output ports purpose.

For monitoring purposes we require a second output of the selected source. In a single channel or master configuration this would be the RF input signal from the local oscillator. In a slave configuration the selected source would be the auxiliary input of the 3-way power divider. This can be implemented with a 2-way power divider, where the input port is connected to the auxiliary output of the 3-way power divider. Port 2 of the 2-way power divider will then provide an output for the monitoring purposes and port 3 will be the RF input signal for the following channels (Figure 3.8).

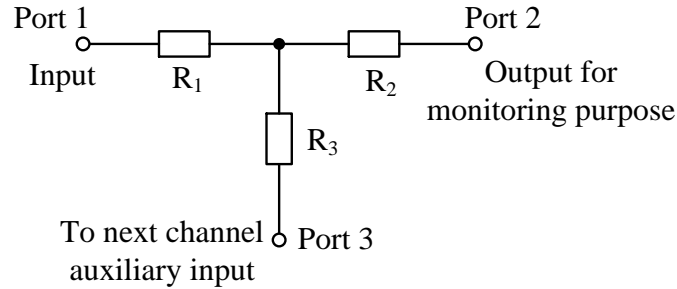


Figure 3.8. 2-way power divider showing the input and output ports purpose.

The frequency of operation is ISM band, from 2.4 - 2.5 GHz centered at 2.45 GHz. The power dividers which are to be prototyped will be part of this thesis work. The design goals of 3-way and 2-way power dividers are shown in Table 3.1. Commercially available 2-way and 3-way resistive power dividers specifications are presented in Table 3.2. The insertion loss of 2-way resistive power divider presented in [35] is 6.5 dB and 3-way divider in [37] is 9.5 dB.

3.3 Small-Signal RF Amplifiers

An amplifier is an active device that is designed to performs the amplification of the voltage, current or both. Based on the frequency of the operation, the amplifiers are categorized. They are DC amplifiers which operate at zero frequency, low frequency amplifiers (audio), and high frequency (RF) amplifiers. Low frequency and high

Table 3.1. *Design goals of the 3-way and 2-way power dividers.*

Parameter	3-way			2-way			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency		2.45			2.45		GHz
Return Loss	15			15			dB
Insertion Loss			9.5			6.0	dB

Table 3.2. *Commercially available 2-way and 3-way power dividers.*

Source	Parameter	Range	Unit
[35]	Frequency	DC-4	GHz
	Insertion Loss	6.5	dB
[36]	Frequency	DC-18	GHz
	Insertion Loss	6	dB
[37]	Frequency	DC-4	GHz
	Insertion Loss	9.5	dB

frequency amplifiers are also termed as AC amplifiers. In AC amplifiers, the small amplitude input signal controls the large DC bias current. The typical performance parameters which describe the amplifier's performance are: power gain, input and output return loss, gain compression, bandwidth of operation, power consumption, and linearity [13].

RF amplifiers are roughly classified into two categories: linear and non-linear amplifiers. If there is a fixed ratio between the input and output at any time then the amplifier is said to be linear amplifier. If the ratio is not fixed, the amplifier is considered as non-linear amplifier. In other words, the amplifier, which preserve the shape of the input signal at the output is called linear amplifier. The amplifiers which can be modeled with linear S -parameters when the input signal amplitude is small and the output signal amplitude varies in proportion to the input are small-signal amplifiers [38]. The linear amplifiers operates with small-signals. The factors which could possibly alter the ratio are the input signal power, frequency, biasing conditions. Depending on the configuration, linearity, and efficiency small-signal RF amplifiers are subdivided into different classes of amplifiers, for example, class A, class B, and class AB. Out of which class A amplifiers are the more linear amplifiers, disadvantages of these are, that they are on contrast these are that they are the least efficient amplifier class.

3.3.1 Amplifier Configurations

There are multiple amplifier configurations where each one has its own advantages and disadvantages. Depending on whether the base, emitter or collector terminal is connected to the ground of an amplifier three configurations are possible. They are

common-base (CB), common-collector (CC), and common-emitter (CE) configurations. In the first one, the input signal is injected between the emitter and ground and amplified version of the input signal is provided between the collector and base terminals. It is widely preferred configuration in realizing the high power and voltage amplifiers. In the CC configuration, the input signal that is to be amplified is applied between the base and collector terminal and the output is provided between the emitter and collector terminals. The CC configuration has high input and low output impedance. It is commonly used for current amplification applications and least preferred for voltage amplifications. More often it is used as buffer amplifier or as an active impedance transformation circuit.

Finally, CE configuration (Figure 3.9) employs the input signal is fed into the base, and the output connected at the collector. It is the most frequently used configuration in almost all electronic circuits. Unlike, the other two configurations, the CE configuration provides both current and voltage amplification and this makes it the first choice in power amplification applications. It is commonly used at radio frequencies [13].

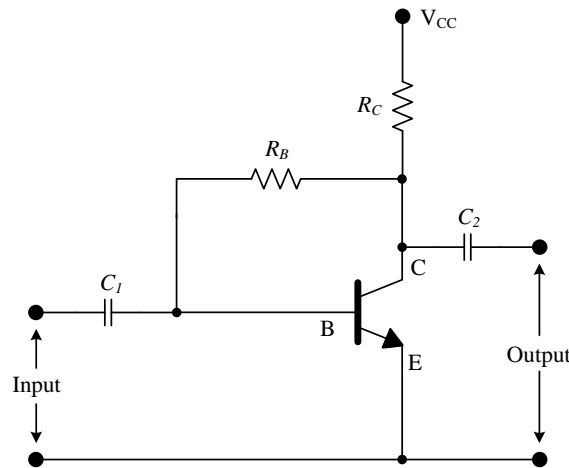


Figure 3.9. Common-emitter amplifier configuration.

3.3.2 RF Amplifier Design Methods

Design and development of an RF amplifier for a particular application requires the designer to follow certain steps or procedures. The basic steps that are followed in almost all design processes are selection of a particular transistor, DC bias point selection, stabilization, and the input and output matching networks. Still, the designer has the choice to assign the priority to the steps. There are numerous textbooks and publications available today that describe the detailed step-by-step design procedure of the RF amplifier. The design procedures described in five different books are summarized below.

In [15] the author Gonzalez describes that a microwave amplifier design is a procedure that is dependent on certain design goals and S -parameters of the transistor. In the author's perspective, the design starts with a set of specifications and the selection of the transistor. Then it follows the unconditional stabilization of the transistor by utilizing the mathematical calculations and graphical techniques. Further, it follows finding the suitable matching networks according to design requirements. And, also the author claims that the DC bias circuit is the least considered one in microwave amplifier design. Nevertheless, the author expresses that the designer should not compromise the amplifier's performance by selecting a poor DC bias circuit. The theoretical concepts required during development of radio frequency amplifiers are outlined in detail in [15] along with example designs.

A step-by-step design procedure of a class A amplifier is presented in [13] by the author Syre. The vital steps are described as follows:

- Selection of suitable transistor based on performance parameters such as, frequency, gain, and availability of the S -parameters files for DC bias currents, and cost.
- Selection of the right bias point by studying the transistor data sheet with which the performance characteristics can be achieved.
- Transistor stability check by inserting the S -parameters model from low to high frequencies from the S -parameter file.
- Making the amplifier unconditionally stable with the necessary steps by checking the stability factor k .
- Designing of the input and output matching networks according to the design requirements.
- Adding the lumped and distributed component models and the substrate properties.

A three step procedure of an amplifier design described by Vendelin [32] is as follows:

1. DC Design.
2. RF Design.
3. Schematic and Layout design.

The author's prime focus is on the selection of the proper DC bias point and bias circuit design. Furthermore, the author describes the relationship between the DC bias current and the RF design. In addition, the author recommends using a curve tracer in the DC bias circuit design. Three different biasing networks, such as,

four resistors, active bias, and active bias with diode are explained in [32]. Further, the author compares the performance of these three bias circuits with respect to the temperature and also performance enhancements. The design of a single stage amplifier for different requirements like, high-gain, maximum available gain, and unilateral gain design is also presented.

Chang presented the step-by-step design procedure of a small-signal amplifier. It is given in [39]. Out of which, the essential steps are described below:

- Tabulate the list of performance requirements. For instance, frequency band of operation, power gain, return loss, OIP3.
- Selection of an active device that suit best for the application.
- Obtain the S -parameters from the vendor or by performing measurements.
- Analyze the minimums and maximums of the active device performance parameters.
- Perform the stability check and make it stable with the necessary steps if it is unstable.
- Examine constant gain circles on the Smith chart.
- Compute maximum or desired power gain of the amplifier.
- Design the input and output matching networks to meet the performance requirements.

The last author Bowick [18] claims that the DC bias circuit should be given the highest priority. Different possible passive DC bias circuits are explained in this book along with the examples. The design of a RF small signal amplifiers with both S - and Y -parameters are also presented. Further, the design of an amplifier for different goals such as, maximum gain or specified gain is also described. The design method of a simultaneous conjugate match and a specified gain is also described. All the procedures are presented with suitable design examples. This could serve as a good reference for the RF amplifier design.

Almost all of the above authors follow the similar procedure in stabilization and power gain estimations, but, with different priorities with respect to the bias circuits, lumped components, and layout constraints. For instance, in [13] the author's emphasizes on the inclusion of the resistive lumped components and the substrate properties in order to achieve the real performance parameters. Further, in [32] the author, Vendelin pays attention to the layout design as a part of the design procedure. Vendelin and Bowick in contrast to Gonzalez give higher priority to the DC bias circuit.

In this thesis work our goal is to design a small-signal RF amplifier for a specified gain. Therefore we discuss in more detail the specified gain design procedure in the following section.

3.3.3 RF Amplifier Design for a Specified Gain

In some applications the gain of the amplifier should be less than the maximum possible gain for that particular transistor in order to have a wide band of operation and/or to provide an exact required specified gain without distortion. This can be achieved with the input and output matching network design. Meaning that, by introducing mismatch on purpose the gain is reduced to the desired gain. This is termed as selective-mismatching [18], [23].

It is accomplished by plotting the constant-gain circles on the Smith chart to represent Γ_s and Γ_L which gives a constant source gain, G_S , and load gain, G_L . For simplicity let us consider a unilateral device which means $|S_{12}|=0$. Detailed description for bilateral case is in [23], [32]. Then the expression for G_S and G_L can be described as

$$G_S = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2}, \quad (3.17)$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}. \quad (3.18)$$

If, $\Gamma_s=S_{11}^*$ and $\Gamma_L=S_{22}^*$ then maximum values of equations (3.17) and (3.18) are given by

$$G_{Smax} = \frac{1}{1 - |S_{11}|^2}, \quad (3.19)$$

$$G_{Lmax} = \frac{1}{1 - |S_{22}|^2}. \quad (3.20)$$

With the simplification procedure given in [22], the center and radius of the source or input constant gain circle is given by

$$C_s = \frac{g_s S_{11}^*}{1 - (1 - g_s)|S_{11}|^2}, \quad (3.21)$$

$$R_s = \frac{\sqrt{1 - g_s}(1 - |S_{11}|^2)}{1 - (1 - g_s)|S_{11}|^2}. \quad (3.22)$$

Similarly, the center and radius of the output is given by

$$C_L = \frac{g_L S_{22}^*}{1 - (1 - g_L)|S_{22}|^2}, \quad (3.23)$$

$$R_L = \frac{\sqrt{1 - g_L}(1 - |S_{22}|^2)}{1 - (1 - g_L)|S_{22}|^2}, \quad (3.24)$$

where, g_s and g_L are the normalized source and load factor given in [23].

The center of the each circle (input and output) lies on the line given by the angle of S_{11}^* and S_{22}^* . The values of Γ_s and Γ_L are selected along these circles. There can be many possible values for Γ_s and Γ_L . With values selected closer to the Smith chart center, the mismatch can be reduced and also the bandwidth can be improved (see Section 2.2).

3.4 17 dB Gain Small-Signal RF Amplifier Design Goals

The small-signal RF amplifier developed in this thesis work is used for the re-design of the SSB. This small-signal RF amplifier is used to compensate the loss introduced by both the 3-and 2-way power dividers, and the cable loss in case of a multi channel configuration (about 1 dB). The minimum loss introduced by the 3-way power divider is roughly 9.5 dB and for the 2-way power divider is 6 dB. The total loss would be 15.5 dB. By taking the cable and connector loss of approximately 1 dB (in a multi channel configuration) into consideration, the total loss would be roughly 17 dB. So, in order to recover the signal loss of 17 dB, the gain of the amplifier is targeted to be 17 dB.

In this application, the required power at the output of the 2-way power divider is 5 dBm [6]. Instead of compensating loss at every output port we decided to make up the loss before the power is even inserted into the 2-way power divider. This way we can compensate the loss of the two ports with only one amplifier. Therefore the desired input signal which is specified at 5 dBm should be already amplified by the same amount as the loss the 2-way power divider introduces, which is 6 dB. This would mean that the amplifier should be capable of driving a signal with a power level of 11.5 dBm. To have more spare headroom the targeted output power is 12 dBm. It should be noted that one goal also is to keep the power dissipation as low as possible to make sure the amplifier does not heat up the other components in the SSB. Also, the operating voltage of the amplifier should be 3.3 V because of the available power supply in the SSB.

The other important design goals of small-signal RF amplifier are listed in Table 3.3. The overall cost of the amplifier is described by the cost of components that are necessary for its reliable operation. The inductors and transistors are more expensive components in amplifiers than resistors and capacitors [40]. Thus by using the least possible number of transistors and inductors the cost of the design can be kept low. To design an RF amplifier with the design goals in Table 3.3 with only one transistor, is proved to be a challenging task. The design and development of this 17 dB small-signal RF amplifier is one part of this thesis work. The design process is presented in Chapter 4.

Table 3.3. *Design goals of the 17 dB gain small-signal RF Amplifier.*

Parameter	Min.	Typ.	Max.	Unit	Notes
Center Frequency		2.45		GHz	
Bandwidth	100			MHz	2.4 - 2.5 GHz
Gain		17		dB	
Gain Flatness	± 0.5			dB	
Input Return Loss	10			dB	
Output Return Loss	15			dB	
Output 1-dB Gain Compression Point	12			dBm	
Voltage		3.3		V	
Stability					Unconditionally Stable

3.5 10 dB Gain Small-Signal RF Amplifier Design Goals

The primary purpose of this amplifier is to compensate the loss introduced by the 3-way power divider. Hence, the gain of the amplifier is targeted to be 10 dB.

The design goals of the 10 dB gain RF amplifier are shown in tabulated 3.4. To make up the power loss of the 3-way divider the output power of the amplifier is specified as 6 dBm, also allowing some headroom. This will give more flexibility in selecting RF input signal power levels. With 6 dBm output power, the amplifier can operate in the linear region even when pushing the local oscillator power levels to its maximum limits. To prototype an RF amplifier with the design targets as specified in Table 3.4 is quite a challenging task. The design approach is presented in Chapter 4. The designed and development of this RF amplifier is a part of this thesis work.

Table 3.4. *Design goals of the 10 dB gain small-signal RF Amplifier.*

Parameter	Min.	Typ.	Max.	Unit	Notes
Center Frequency		2.45		GHz	
Bandwidth	100			MHz	2.4 - 2.5 GHz
Gain		10		dB	
Gain Flatness	± 0.5			dB	
Input Return Loss	10			dB	
Output Return Loss	15			dB	
Output 1-dB Gain Compression Point	6			dBm	
Voltage		3.3		V	
Stability					Unconditionally Stable

4. IMPLEMENTATION

This chapter describes the design and fabrication of power dividers and amplifiers. This chapter is organized as follows, the first section gives the detailed description of the design process of 3-way resistive power divider followed by 2-way resistive power divider in the second section. The third section presents the design process of the 17 dB gain RF amplifier which includes, selection of transistor, DC bias circuit design, stabilization, and matching network design. The simulation and measurement results are also covered. In Section 4.4 the 10 dB gain RF amplifier design process, simulation, and measurement results are presented.

4.1 3-way Power Divider

4.1.1 Design Process

The T-junction resistive power divider topology was chosen for the design. The 3-way resistive power divider is a four-port device; one input port and three output ports ($N=3$) ports. The divider will have four resistors at four ports of the same value. The calculated resistor value from the equation (3.15) by substituting $N=3$ and characteristic impedance, Z_0 , of $50\ \Omega$ is $25\ \Omega$. The calculated $25\ \Omega$ resistors are not available in the lab instead we have selected $24\ \Omega$ resistor which is the only available closest value. The layout of the 3-way resistive power divider with $24\ \Omega$ resistors at each port is shown in Figure 4.1. The impedance seen at P1 by looking at P2, P3, and P4 with matched terminations is $48.67\ \Omega$ which is close to $50\ \Omega$. The insertion loss of the 3-way resistive power divider calculated from the equation (3.16) is 9.5 dB.

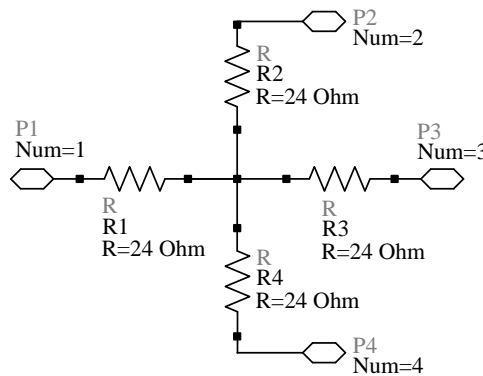


Figure 4.1. 3-way resistive power divider layout diagram.

4.1.2 Simulation Results

The simulations of the 3-way resistive power divider were carried out within Agilent Technologies ADS 2011.10 with the schematic shown in Figure A.1 in Appendix A. ADS is a Computer Aided Design (CAD) tool used for RF and microwave simulations [41]. S -parameter simulations were performed with the ideal components to determine the performance of the divider from 2.3 GHz through 2.6 GHz. The real component models were not available in ADS library.

Figure 4.2 shows the simulations reflection loss results at four-ports. It is clear from the figure that, a minimum return loss of 24.9 dB is available in the operating frequency band 2.4 - 2.5 GHz at all four-ports. The 3-way power divider was designed for the source and load impedance of $50\ \Omega$. For perfect matching conditions the source and load impedance should have real part of $50\ \Omega$ and imaginary part of $0\ \Omega$. However, values closer to them are sufficient.

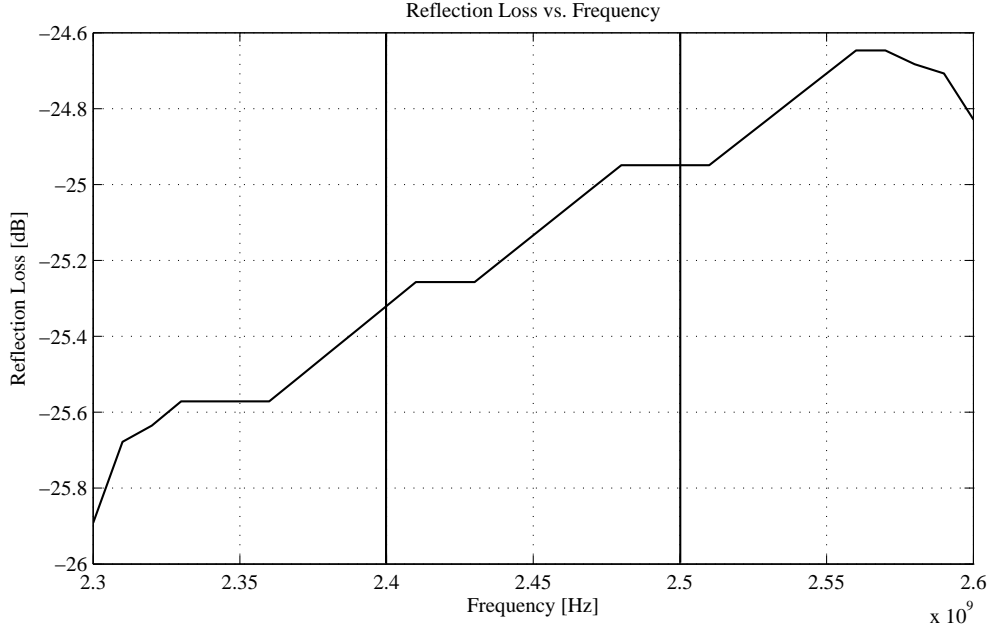


Figure 4.2. Simulated reflection loss of the 3-way resistive power divider at four-ports versus frequency.

The simulations transmission loss results are shown in Figure 4.3. Simulations shows that the insertion loss of the 3-way resistive power divider is approximately 9.55 dB which is close to the calculated value of 9.5 dB. The frequency of interest is highlighted with dark vertical lines.

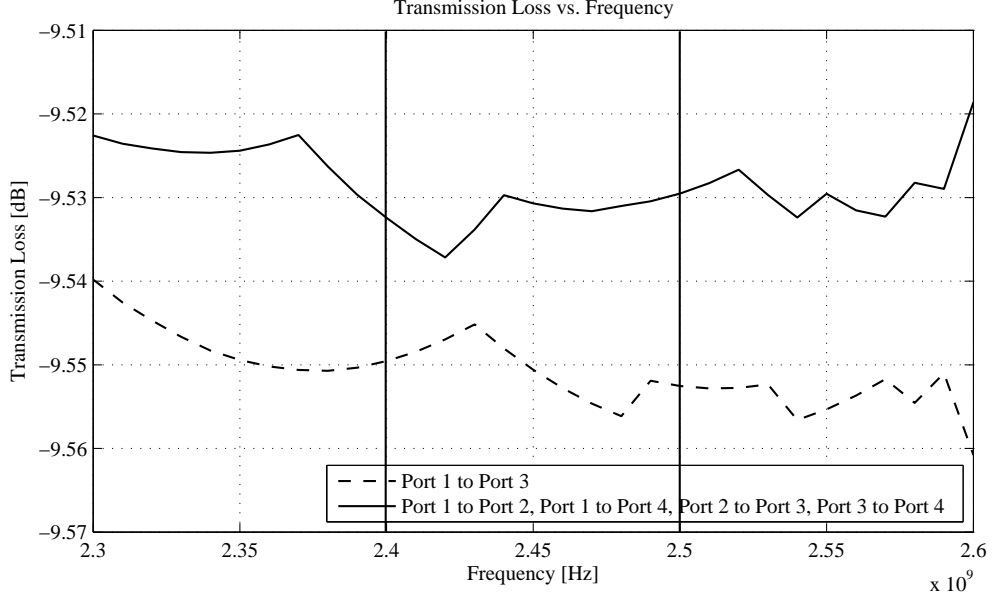


Figure 4.3. Simulated transmission loss of the 3-way resistive power divider versus frequency.

4.1.3 Layout and Fabrication

The layout of the 3-way resistive power divider (Figure 4.4 (a)) was created in ADS from the final schematic shown in Figure A.1 in Appendix A.1. The Rogers Corporation's double sided RO4350 LoPro, 30 mil [42] substrate was used. The substrate permittivity of $\epsilon_r=3.66$, thickness of the copper is 33 μm , and height of the substrate is 0.762 mm. The milling machine, ProtoMat S63 advanced circuit board plotter [43] was used for milling the PCB. The divider is fabricated and prototyped in RF Laboratory at NXP Semiconductors. The Rogers Corporation MWI-2010 calculator [44] was used for calculating the strip line (MCROSO and CPW) dimensions for realizing 50 Ω impedance. The top and bottom layer ground planes are connected through the via holes of 0.25 mm diameter. The board has dimension of 20.45 \times 20.45 mm. The resistors used are of size 0402, E24 series from Yageo vendor. Figure 4.4 (b) shows a photograph of the assembled 3-way resistive power divider with SMA-female connectors at four-ports for the input and output of the RF signals.

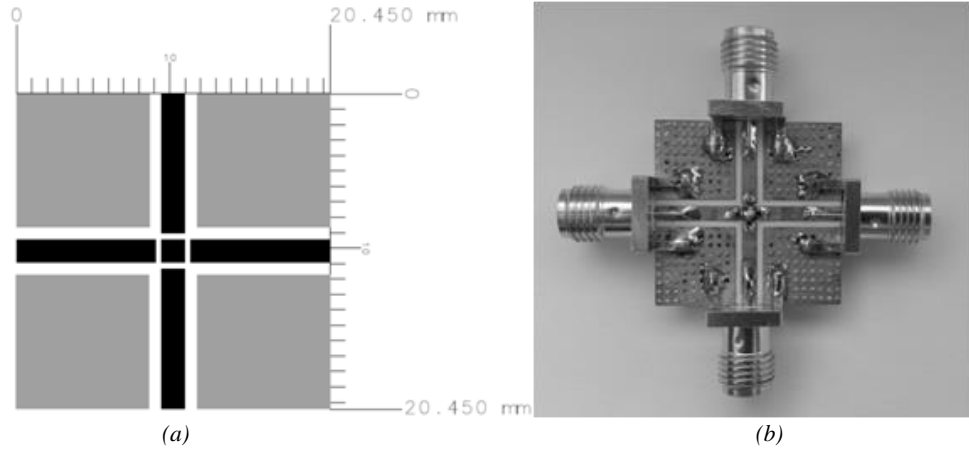


Figure 4.4. 3-way resistive power divider: (a) Top layer of the layout; Gray portion: Ground plane, Dark portion: RF Signal path, (b) Photograph of the prototyped power divider.

4.1.4 Measurement Results

The measurements and simulations reflection loss at four-ports of the 3-way resistive power divider are shown in Figure 4.5. Both results are presented in the same graph to ease the comparison. The measured and simulated return loss at center frequency of 2.45 GHz is approximately 23 dB and 25.2 dB respectively. The transmission loss between the ports of the divider is shown in Figure 4.6. The measured insertion loss at center frequency of 2.45 GHz is approximately 9.88 dB.

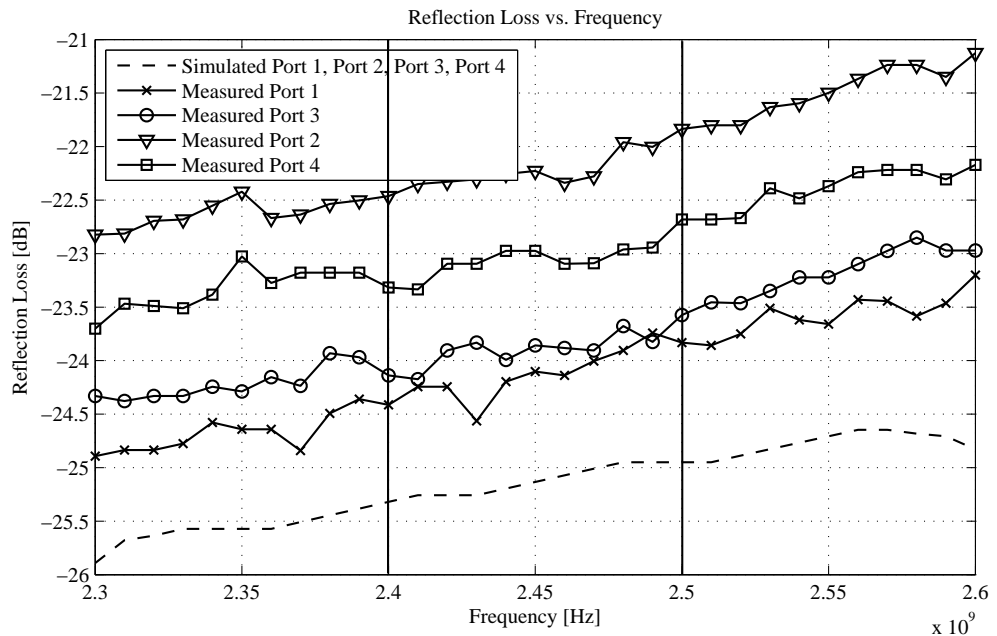


Figure 4.5. Measured and simulated reflection loss of the 3-way resistive power divider versus frequency.

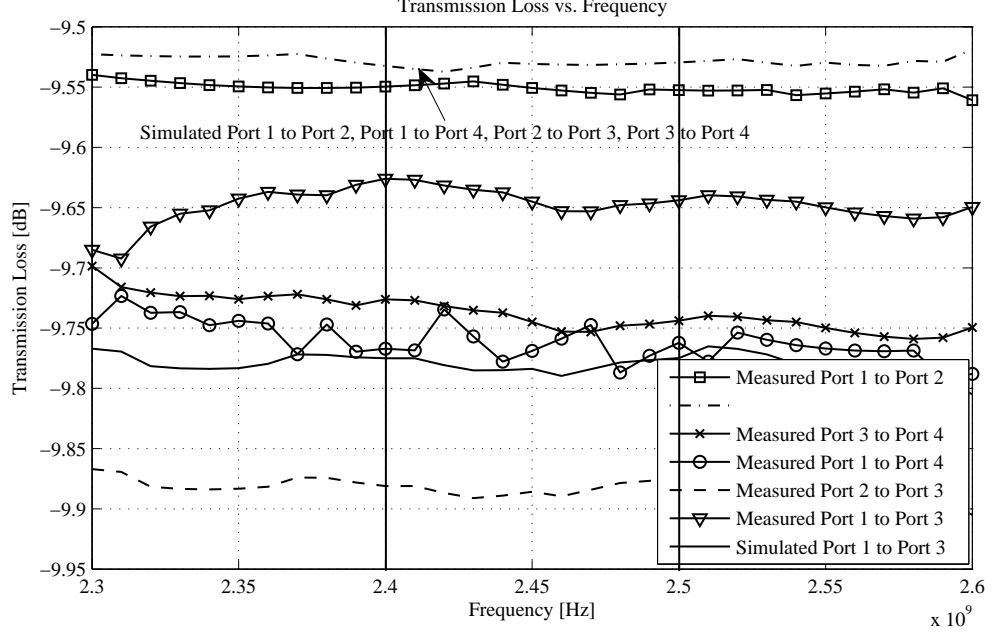


Figure 4.6. Measured and simulated transmission loss of the 3-way resistive power divider versus frequency.

4.2 2-way Power Divider

4.2.1 Design Process

Like for 3-way resistive power divider, the T-junction power divider topology chosen for this design also. The 2-way resistive power divider is a three-port device, one is input port and two are output ($N=2$) ports. This will have three resistors of the same value of 16.6Ω calculated from the equation (3.15). The calculated 16.6Ω value resistors are not available in E24 series. The 16Ω resistor is the closest value to 16.6Ω that exists are used in the fabrication. The insertion loss calculated from the equation (3.16) is 6.0 dB. With 16Ω resistor the impedance seen at P_1 by looking at P_2 and P_3 with matched terminations is 49Ω . The layout of the 2-way resistive power divider is shown in Figure 4.7 with 16Ω resistors at each port.

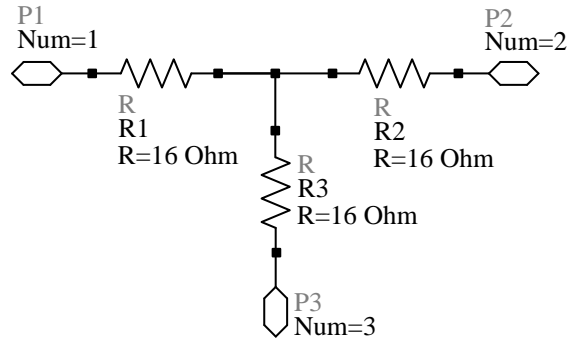


Figure 4.7. 2-way resistive power divider layout diagram.

4.2.2 Simulation Results

The S -parameter simulations of the 2-way resistive power divider are performed in ADS with the schematic shown in Figure A.2 in Appendix A. Simulations reflection loss results at three-ports are shown in Figure 4.8 and it is clear from the figure that return loss of 24.8 dB is available in 2.4 - 2.5 GHz frequency band. Like 3-way power divider, the 2-way power divider was also designed for the source and load impedance of 50 Ω .

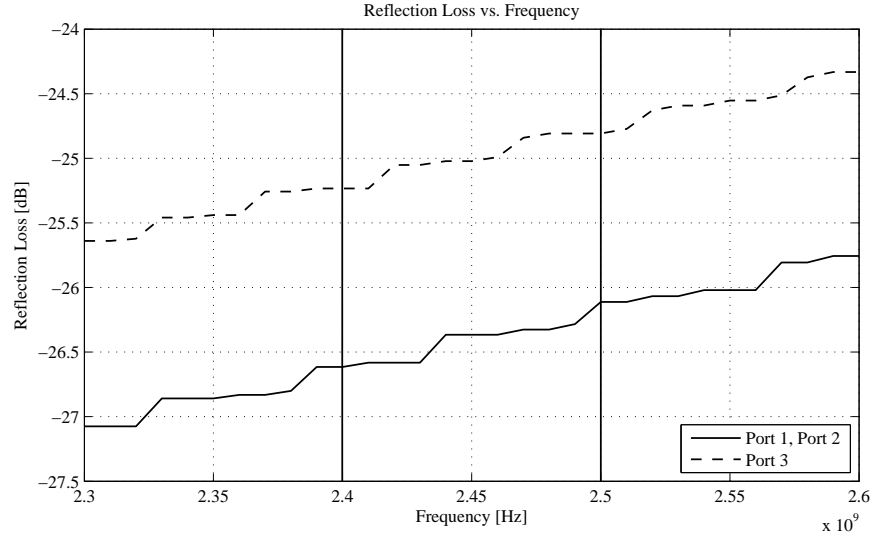


Figure 4.8. Simulated reflection loss of the 2-way resistive power divider at three-ports versus frequency.

The simulated transmission loss of the 2-way resistive power divider is shown in Figure 4.9. Simulated insertion loss is 6.07 dB at 2.45 GHz and is almost same as calculated value of 6.0 dB.

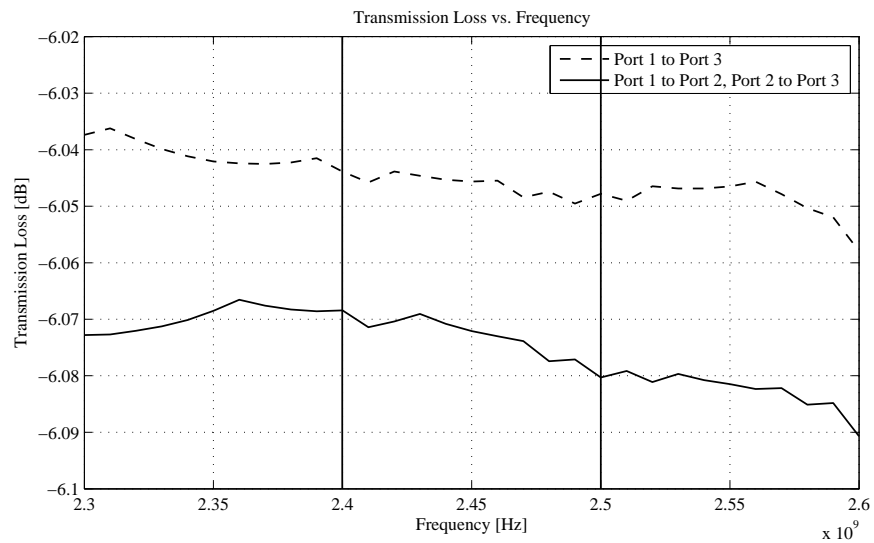


Figure 4.9. Simulated transmission loss of the 2-way resistive power divider versus frequency.

4.2.3 Layout and Fabrication

The layout shown in Figure 4.10 (a) was generated in ADS with the schematic shown in Figure A.2 in Appendix A. The same PCB material that is used for 3-way power divider is also used for this 2-way power divider. A similar procedure as in 3-way power divider was followed in calculating the dimensions, milling, and fabrication. The PCB board has dimension of 20.45×16.860 mm. The prototyped 2-way power divider with SMA-female connectors at three-ports is shown in Figure 4.10 (b).

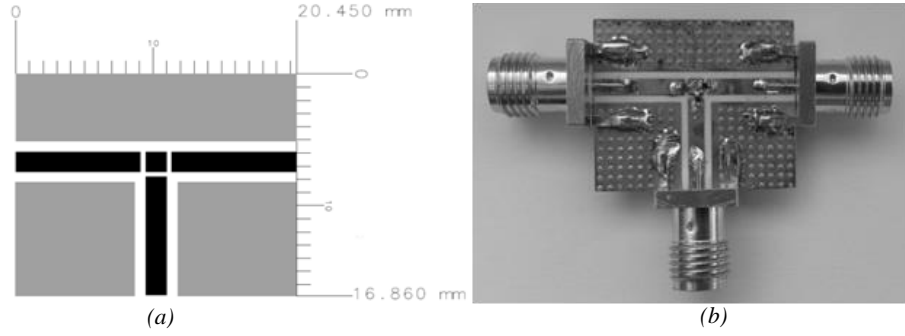


Figure 4.10. 2-way resistive power divider: (a) Top layer of the layout; Gray portion: Ground plane, Dark portion: RF Signal path, (b) Photograph of the prototyped power divider.

4.2.4 Measurement Results

The measurements and simulations reflection loss at three-ports of the 2-way power divider are shown in Figure 4.11. The measured return loss at port 1 and port 2 is 24 dB and 24.2 dB, and at port 3 is 25.6 dB at center frequency. The measured and simulated transmission loss are shown Figure 4.12. The measured insertion loss is close to 6.26 dB at 2.45 GHz.

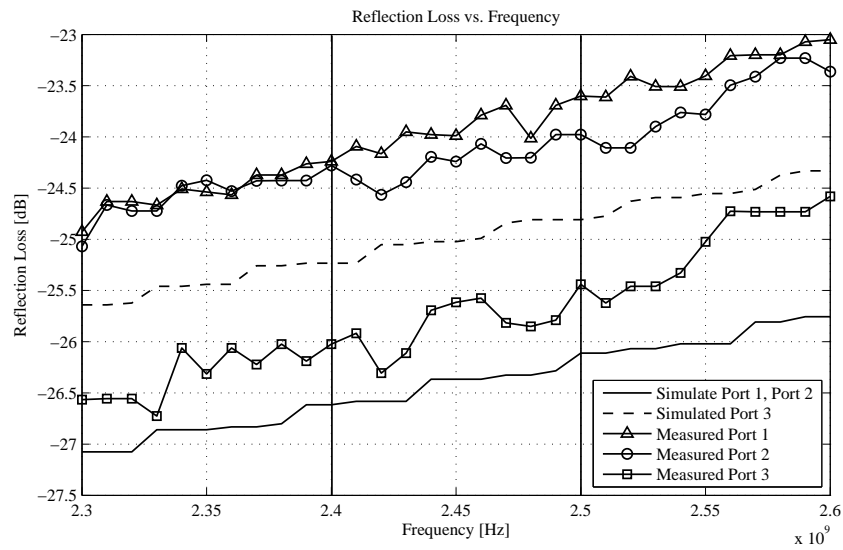


Figure 4.11. Measured and simulated reflection loss of the 2-way resistive power divider versus frequency.

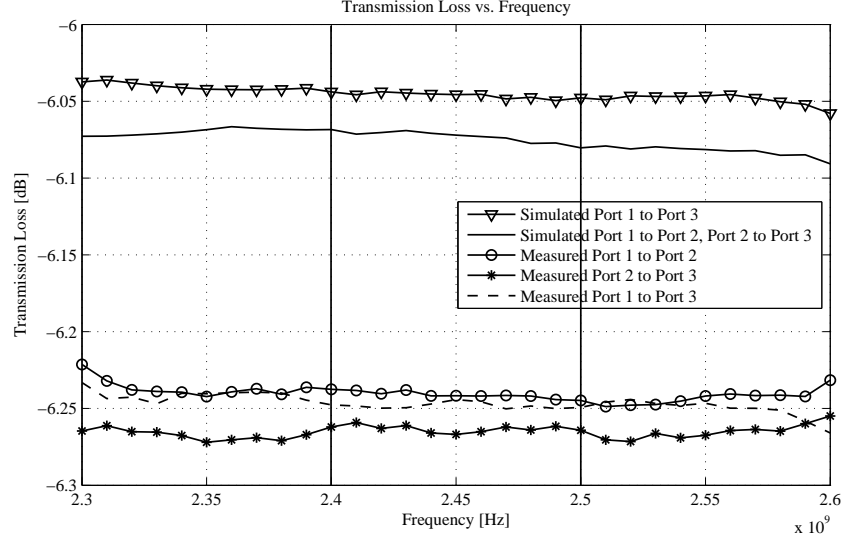


Figure 4.12. Measured and simulated transmission loss of the 2-way resistive power divider versus frequency.

4.3 17 dB Gain Small-Signal RF Amplifier

4.3.1 Selection of Transistor

The most widely used transistor technologies in RF amplifiers is BJTs and field effect transistors (FET) [45]. The performance of the transistor is dependent on the manufacturing process as well as on its internal structure. The BJT and FET technology devices are available with affordable pricing and decent performance parameters with respect to the gain and power consumption. The BJT technology transistors performs well up to 4 GHz [15]. For frequencies higher than 4 GHz the FET technology transistors performs better than the BJT technology. The FETs are more expensive than BJTs [38], [40]. Furthermore, the FETs exhibit higher input and output impedances than BJTs. This brings difficulties in designing of the input and output matching networks [46]. The BJTs are preferred where the cost of the design is an important criterion over the performance at higher frequencies. Because of the above mentioned advantages the BJT technology was chosen for the design.

According to the data sheets, the available RF transistors from the NXP with almost similar performance at the frequency of operation are BFU660F [47], BFU690 [48], and BFU760F [49]. All these three transistors are evaluated in detail in order to select the right transistor with which all the design goals can be achieved. First, these three transistors are made unconditionally stable with a simple stabilization network connected to the models of the transistors at the output and next, are matched with a simple possible matching network. With this arrangement we observed that,

the gain of the transistor BFU760F is close to our desired gain. Moreover, the output impedance is close to $50\ \Omega$ at the frequency of interest. Thus, the transistor BFU760F was selected for the design. Stabilization and matching are performed for a DC operating current of 20 mA and the collector to emitter voltage of 2.5 V.

4.3.2 DC Bias

The two resistor voltage feedback bias circuit was (as discussed in Section 2.5) employed to set the bias current in the transistor BFU760F. Because, it utilizes only two resistors and single power supply. The DC current gain, h_{FE} , of the transistor BFU760F is specified in the range from 155 to 505 [48]. From this wide range it is difficult to define the correct value for a specific DC bias current. The h_{FE} of BFU760F is a function of collector current, I_C , and collector-to-emitter voltage, V_{CE} , and also variations in the manufacturing process (Section 2.5). The acceptable value of h_{FE} was determined with the BJT curve tracer in ADS. From the data sheet it was observed that, with $V_{CE}=2.5\text{ V}$, $I_C=20\text{ mA}$ it is possible to achieve the gain of 17 dB and output 1-dB compression point of 12 dBm.

The obtained value of h_{FE} from the curve tracer is equal to 315 for $V_{CE}=2.5\text{ V}$ and $I_C=20\text{ mA}$. The voltage feedback bias circuit resistor values are calculated with the Ohm's law and with V_{CE} , h_{FE} , and I_C . The calculated bias circuit resistor values are of base resistor $R_b=40\text{ k}\Omega$ and collector resistor $R_c=40\ \Omega$ are shown in Figure 4.13. It is important to mention that, variations in manufacturing process causes variations in h_{FE} from one production to another and it is not possible to estimate in the simulations. Hence, the exact bias current can be tuned with the fabricated prototype if it is necessary.

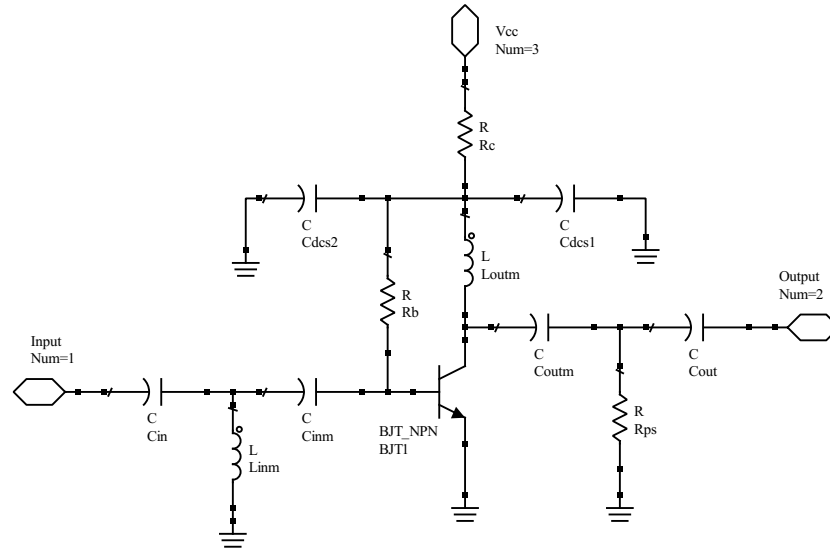


Figure 4.13. Simplified schematic of the 17 dB gain RF amplifier, the description of each component and its optimized values are given in Table 4.1.

In order to keep the component count down the collector current is fed into the transistor through the inductor (L_{outm}) which is a part of the output matching network as well as DC feed (see Section 4.3.3). This inductor allows the DC current to pass through it to reach the collector terminal of the transistor while preventing the RF signal to reach the power supply.

4.3.3 RF Design Process

Once the transistor and DC bias current are selected for the design there are different procedures described in Section 3.3.2 from different authors how to proceed further in the design. The next step in the design is to make the transistor unconditionally stable and achieving the required gain of 17 dB and good return loss with the matching and stability networks. First, we proceed with the stability analysis and then designing of a stability network. Next, the input and output matching networks are designed for achieving the gain and return loss. The design approach followed in this design is similar to the procedure described by Syre [13] and Niknejad [50]. However, we do not strictly follow these procedures and we use our own intuition. In the following subsections, the RF design processes such as, stability, output matching, and input matching are discussed.

Stability

The potential instabilities that are caused by the parasitic effects of the emitter grounding and the transistor itself has to be eliminated for achieving the unconditional stability of the amplifier. For this, the stabilization network was designed according to the procedure given in [15]. This procedure uses resistors connected either to the input or output of the transistor. The values of the resistors were determined with the help of the stability circles plotting on the Smith chart of the reflection coefficient plane. The parasitic effect of emitter grounding was simulated with a small emitter inductor, L_e , of 0.2 nH [20](Appendix B, Figure B.1).

The S -parameter model of the transistor BFU760F (Appendix A, Table A.1) was used to investigate the stability of the transistor. The simulated source and load stability circles of the transistor BFU760F are shown in Figure 4.14. The region outside the stability circle is a stable region (see Section 2.2.3).

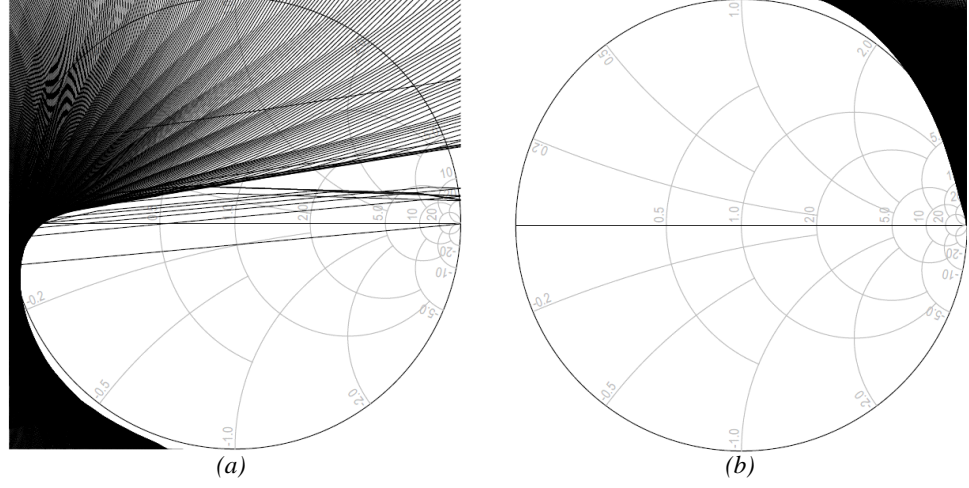


Figure 4.14. Stability circles of the transistor BFU760F: (a) Source stability circle showing the stable region outside the circle, (b) Load stability circle showing the stable region outside the circle.

Figure 4.15 graphically shows the transistor is potentially unstable (μ , μ -prime, and k are less than unity) up to 4.25 GHz. The transistor is potentially unstable in the operating frequency range. The stability circles in Figure 4.14 facilitates to determine the stabilization resistor value and position.

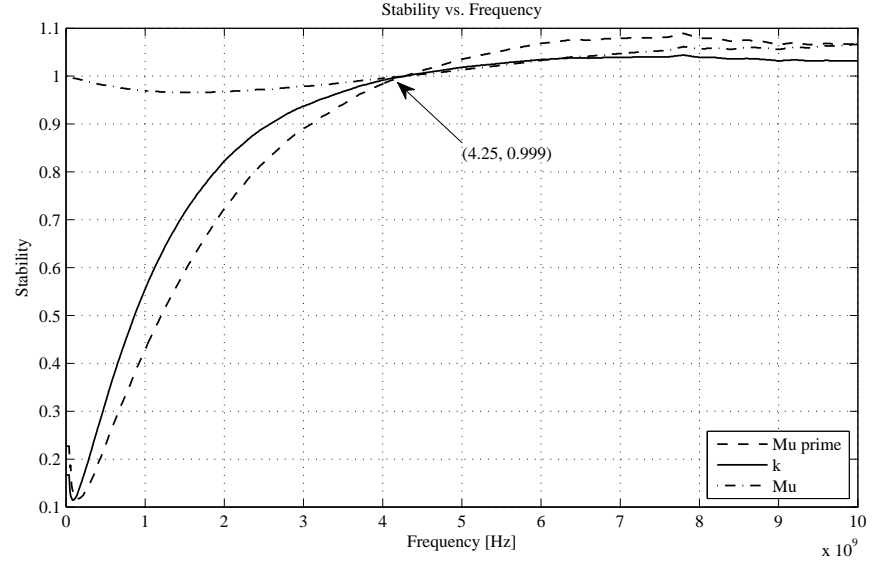


Figure 4.15. Simulated stability factors μ , μ -prime, and k before stabilization showing potentially unstable up to 4.25 GHz.

The unconditional stability of the transistor can be achieved by connecting a high value resistor either in series to the input or parallel to the output. The first possible (series) method is avoided in this design in order to have 50 Ω impedance in the RF signal path and also to avoid the decrease in gain. So, with a parallel resistor $R_{ps}=390 \Omega$, determined from the stability circle, connected to the collector of the

transistor the unconditional stability (μ or μ -prime >1 , $k>1$) was accomplished from DC to 10 GHz as shown in Figure 4.16.

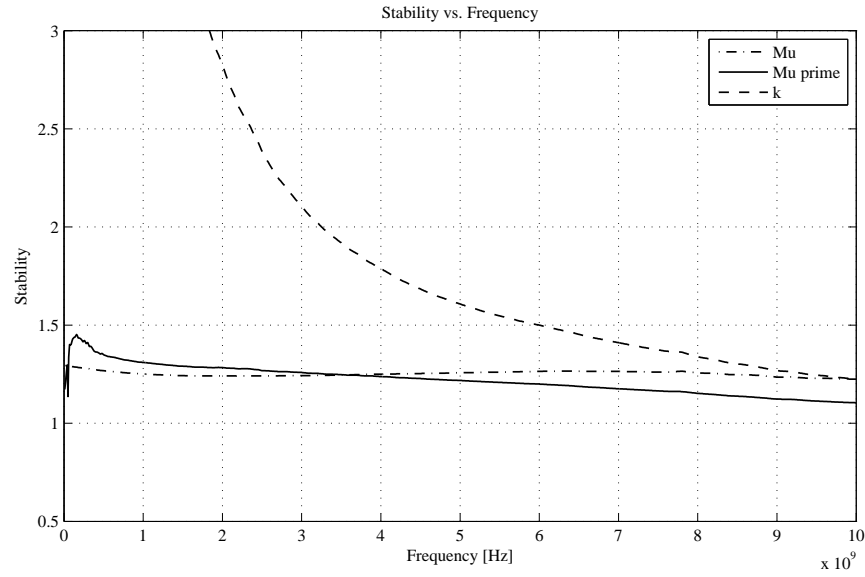


Figure 4.16. Simulated stability factors μ , μ -prime, and k showing transistor is unconditionally stable through 10 GHz.

The schematic diagram used for stabilization is shown in Figure 4.17 along with the parallel stabilization resistor, R_{ps} , at the collector of the transistor and emitter grounding inductor, L_e .

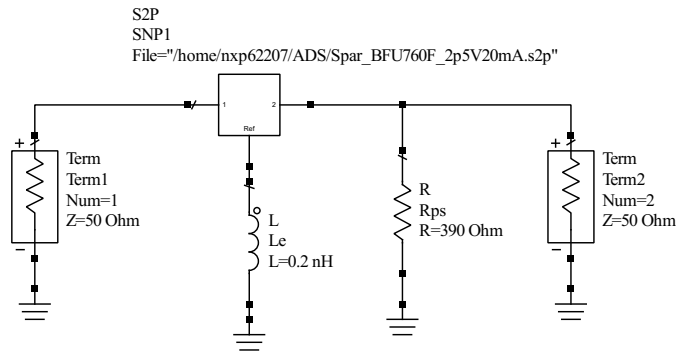


Figure 4.17. Schematic used for the stabilization of the transistor.

Output Matching

Figure 4.18 shows the Smith chart representing the load reflection coefficient plane with the constant gain circles at 2.45 GHz frequency. As it can be observed, matching the 17.5 dB gain circle with the output matching network the desired gain of 17 dB can be achieved. The chosen impedance on the 17.5 dB gain circle which is close to the center of the Smith chart is $Z_{out}=(34.54+j23.48) \Omega$. The output matching network matched the 50Ω impedance to Z_{out} at the operating frequency of 2.45

GHz. The output matching network composed of the parallel inductor $L_{outm}=4.7$ nH and the series capacitor $C_{outm}=11$ pF. The parallel inductor is connected to the ground through a decoupling capacitor, C_{dcs1} , which bypasses the fluctuations in the DC supply voltage. The output matching inductor, L_{outm} , performs the two tasks, as a matching inductor and short for the DC current. The placement of L_{outm} , C_{outm} , and C_{dcs1} are shown in Figure 4.13.

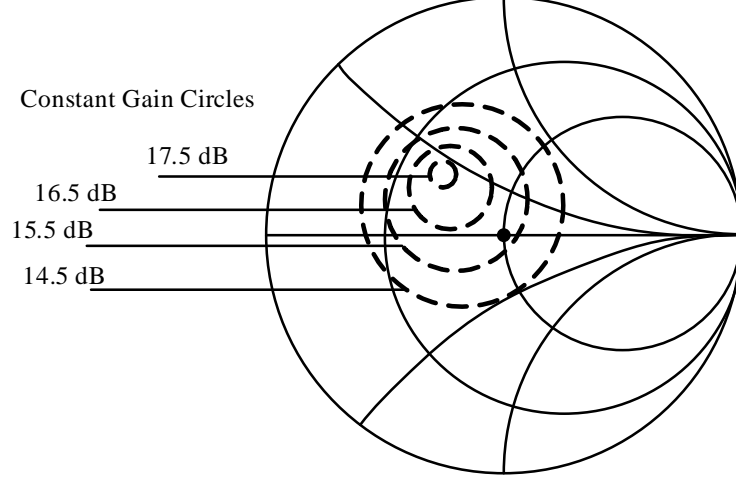


Figure 4.18. Load reflection coefficient plane of the Smith chart with the constant gain circles of the transistor *BFU760F* at 2.45 GHz frequency with an emitter grounding inductor and stabilization resistor.

Input Matching

The input matching network matched the input impedance $Z_{in}=(17.83-j18.23) \Omega$ to 50Ω source impedance with the parallel inductor $L_{inm}=2.8$ nH and the series capacitor $C_{inm}=3$ pF at 2.45 GHz frequency. The shunt capacitor, C_{dcs2} , acts as an open for the DC current and short for the operating frequency signals. The placement of the components can be noticed in Figure 4.13.

4.3.4 Simulation Results

The simulations were performed in ADS with the schematic shown in Figure B.1 in Appendix B. Figure 4.19 shows the simulations input and output reflection loss in the frequency range from 1 GHz through 4 GHz which covers the operating frequency band. The operating frequency band, 2.4 - 2.5 GHz, is highlighted with dark vertical lines. The input return loss at 2.4 GHz and 2.5 GHz is 14.9 dB and 14 dB respectively. The output return loss is 20 dB and 17 dB. If we consider 10 dB return loss is enough for the operation, it is clear from the figure that, the input and output return loss are good enough for the operation in the operating frequency band. The output return loss is better than the input return loss. The Matlab processing software from Mathworks [51] is used for post-processing of the results.

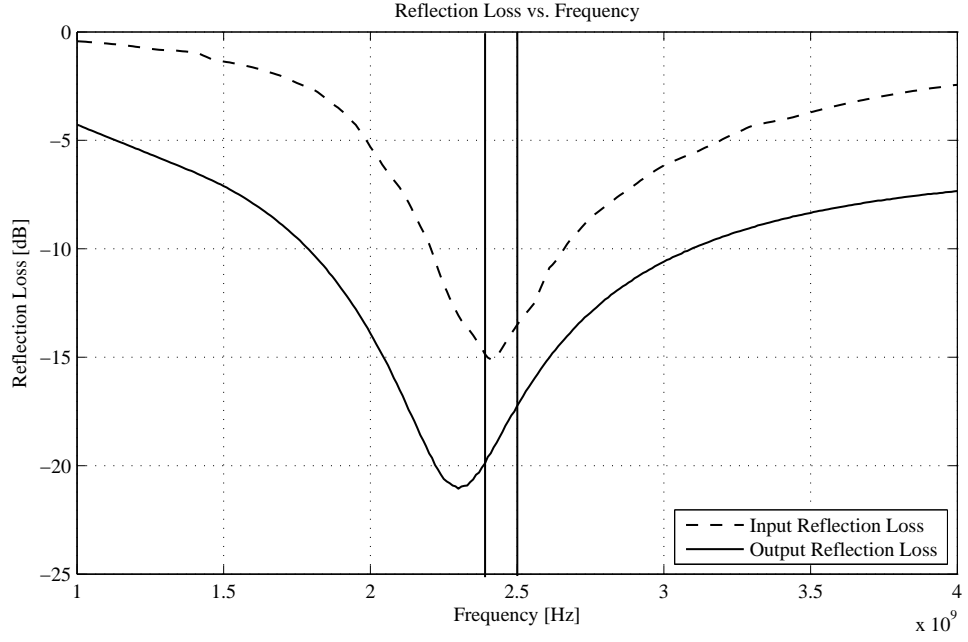


Figure 4.19. Simulated input and output reflection loss of the 17 dB gain amplifier versus frequency.

The simulated gain of the amplifier is shown in Figure 4.20. The wider frequency range was selected for showing the peak in the operating frequency range. The simulated gain is close to 17 dB which is our desired gain at our desired frequency range and the gain flatness is 0.4 dB which is in our specified range.

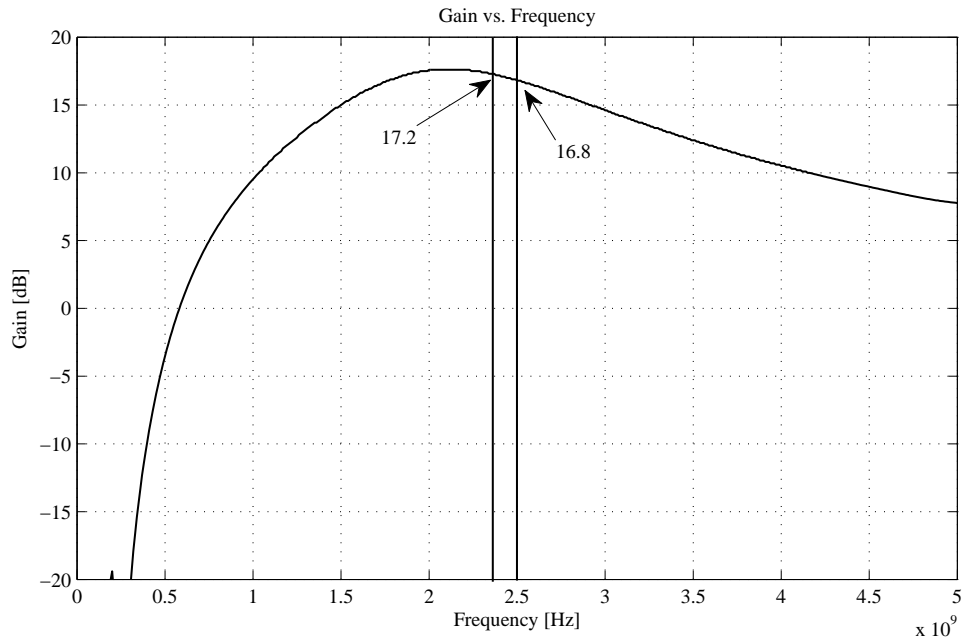


Figure 4.20. Simulated gain of the 17 dB gain amplifier versus frequency.

Harmonic Balance (HB) simulations [52] were performed for computing the output 1-dB gain compression point and OIP3. The simulations result of OIP3 is equal

to 29 dBm with spacing of 1 MHz and output 1-dB gain compression point is equal to 12 dBm at 2.45 GHz frequency.

Table 4.1. List of lumped components used for 17 dB gain amplifier.

Component	Simulated	Optimized	Package	Purpose
R_c	40 Ω	24 Ω	0402	DC bias
R_b	40 k Ω	36 k Ω	0402	DC bias
R_{ps}	390 Ω	390 Ω	0402	Stability
L_{inm}	2.8 nH	2.4 nH	0402	Input Matching
L_{outm}	4.7 nH	4.7 nH	0402	Output Matching and DC feed
C_{in}	100 pF	100 pF	0402	DC block
C_{inm}	3 pF	1.5 pF	0402	Input Matching
C_{out}	100 pF	100 pF	0402	DC block
C_{outm}	11 pF	12 pF	0402	Output Matching
C_{dcs1}	180 pF	180 pF	0402	High Frequency decoupling
C_{dcs2}	10 nF	10 nF	0402	Decoupling

4.3.5 Layout and Fabrication

The layout of the RF amplifier was created in ADS shown in Figure 4.21(a). Rogers RO4350B LoPro, 30 mil [53] substrate of permittivity $\epsilon_r=3.55$, thickness of 33 μm , and height of 0.779 mm was used for the fabrication of the amplifier. The amplifier is fabricated in the RF Laboratory at NXP Semiconductors. Similarly like in power dividers, the milling machine, ProtoMat S63 advanced circuit board plotter was used for milling the PCB. The dimensions of the strip lines (MTEE, MLIN, MCURVE, and CPWG) were calculated with MWI-2010 calculator at 2.45 GHz. The grounding on both sides of the PCB was realized with 0.24 mm via holes. The board has dimension of 24.416 \times 18.759 mm. The Murata lumped components (inductors and capacitors) are used of size 0402. The resistors used are from Yageo vendor of size 0402. The transistor package is SOT343F. A photograph of the fabricated amplifier is shown in Figure 4.21(b) with SMA-female connectors at the input and output of the amplifier for the RF signals. The two emitter terminals of the transistor were grounded. The amplifier circuit consists of 11 passive components and one active component.

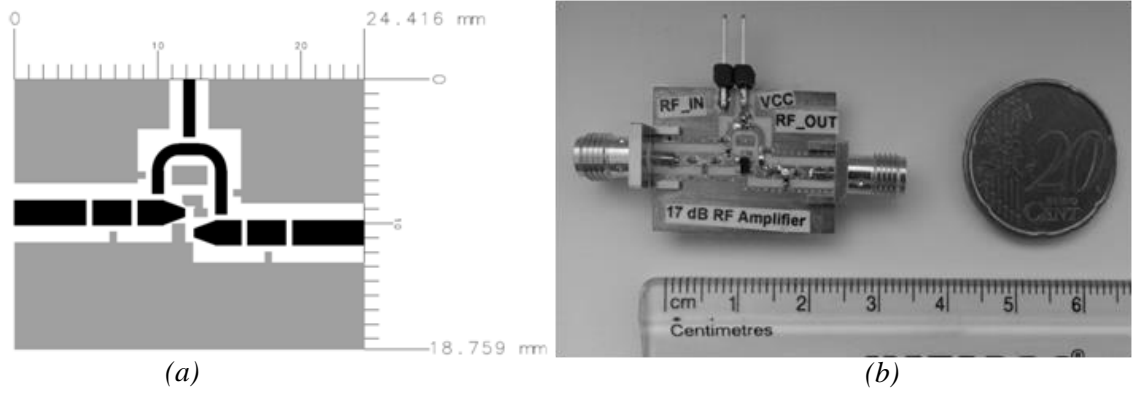


Figure 4.21. 17 dB gain RF amplifier: (a) Layout of the amplifier (Top layer); Gray area: Ground plane, Black area: Signal path, (b) Photograph of the prototyped amplifier along with the top of the twenty-euro cent coin and a ruler.

4.3.6 Measurement Results

The measurements were performed with the fabricated RF amplifier as shown in Figure 4.21(b) in RF Laboratory in RF Small Signal Group at NXP Semiconductors.

The transistor bias current was slightly different than that of simulated due to the variations in transistor manufacturing process. First, the bias resistors, R_c and R_b , were tuned to 24 Ω and 36 k Ω respectively to achieve exactly 20 mA of collector current. The list of lumped components used and their functionalities are detailed in Table 4.1.

A Rohde & Schwarz ZVA21 vector network analyzer (VNA) was used for S-parameters and 1-dB compression point measurements of the amplifier. The VNA was calibrated with the calibration unit beforehand. The measured S -parameters describe gain, return loss, and stability. A FSQ26 signal analyzer and two SMU200A vector signal generators were used for OIP3 measurements.

Figure 4.22 shows the the tuned amplifier measured and actual simulated input and output reflection loss of the amplifier. It should be mentioned that, the input and output matching networks were tuned on the assembled board, the component values can be noticed from Table 4.1. The simulated results are also plotted on the same graph to ease the comparison. Before tuning, the difference between the simulation and measured results of the simulated circuit was 4.6 dB. The deviation of approximately 1.5 dB can be observed between the simulated and tuned amplifier measured results (Figure 4.22) in the operating frequency band. The reasons for this deviation are discussed in Section 6.2. The measured and simulated gain of the amplifier are shown in Figure 4.23. As it can be seen from the figure that, the simulated and measured gains are almost same. The simulated and measured stability (from VNA) of the amplifier from 0 to 10 GHz is shown in Figure 4.24. The comparison of design goals, simulations, and measurements results are shown

in Table 4.2.

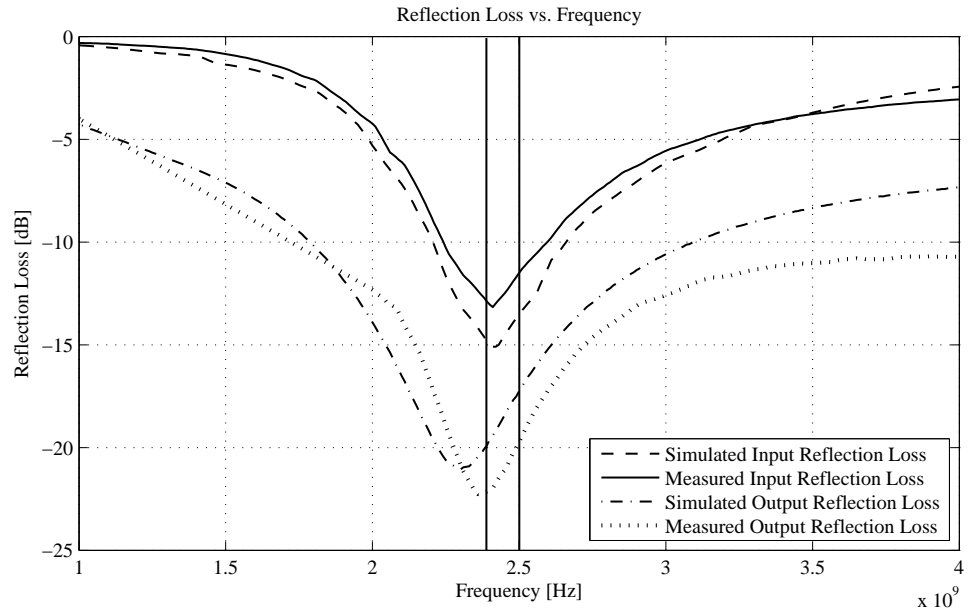


Figure 4.22. Tuned amplifier measured and actual simulated input and output reflection loss of the 17 dB gain amplifier versus frequency.

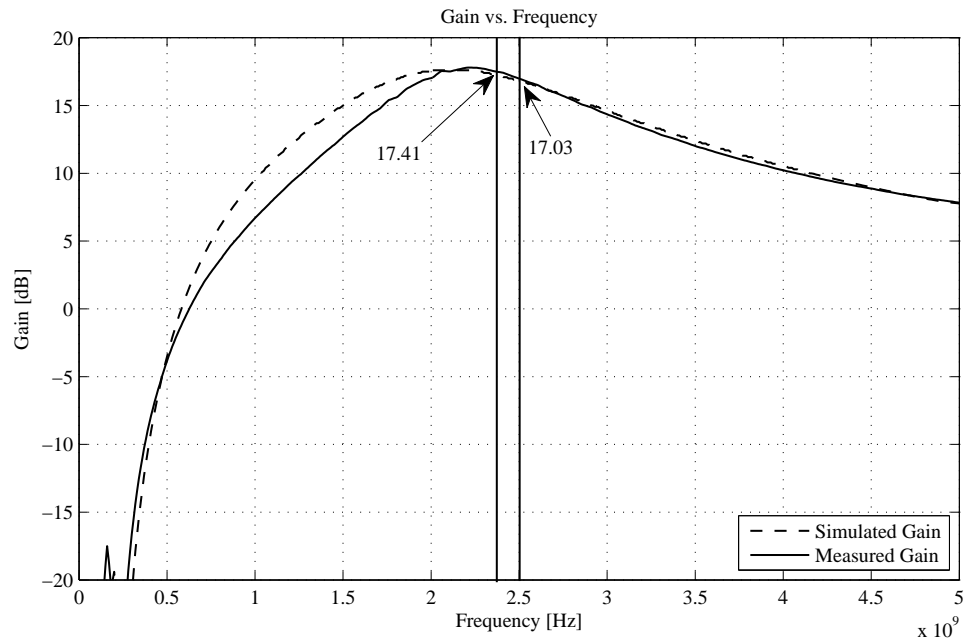


Figure 4.23. Measured and simulated gain of the 17 dB gain amplifier versus frequency.

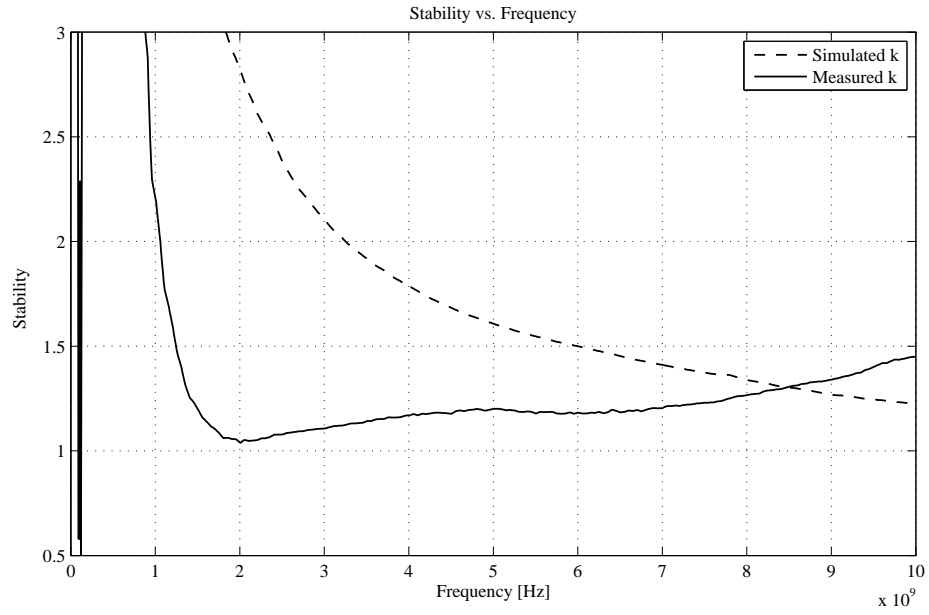


Figure 4.24. Measured and simulated stability factor k of the 17 dB gain amplifier versus frequency.

Table 4.2. Comparison of design goals, simulations, and measurements of 17 dB gain amplifier at 2.45 GHz.

Parameter	Design goals	Simulations	Measurements	Unit	Notes
Supply Voltage	3.3	3.3	3.3	V	
Supply Current	-	20	20	mA	
Center Frequency	2.45	2.45	2.45	GHz	
Bandwidth	100	320	310	MHz	2.4-2.5 GHz, RL > 10 dB
Gain	17	17.1	17.2	dB	
Gain Flatness	± 0.5	± 0.4	± 0.3	dB	
Input Return Loss	10	14.5	12.5	dB	
Output Return Loss	15	19.5	21.5	dB	
Reverse Isolation	-	23.5	23.5	dB	
Output 1-dB Gain Compression Point	12	12	11.4	dBm	
OIP3	-	29	29	dBm	
Stability					Unconditional Stability
Price	-	-		1.5	€

4.4 10 dB Gain Small-Signal RF Amplifier

4.4.1 Selection of Transistor

For this design we have followed the similar procedure like in 17 dB amplifier in the selection of transistor for the design. The transistor BFU760F was further evaluated in selecting the suitable bias current at which the design goals are possible to achieve. We noticed that, at 20 mA bias current, collector to emitter voltage of 2.5 V with series and parallel resistor stabilization network the gain was close to the desired gain of 10 dB with a acceptable return loss. The other bias currents resulted in gain lower or higher than the desired gain which makes the matching network more complicated.

Hence, we decided to use transistor BFU760F for this design as well. The other significant advantages of using the same transistor are that the previous bias circuit can be re-used and also the total time spent on designing the bias circuit and whole design can be brought down considerably. Moreover, the same layout can be re-used with necessary modifications. The DC bias design procedure was same as described in Section 4.3.2. The simplified schematic of the amplifier is shown in Figure 4.25.

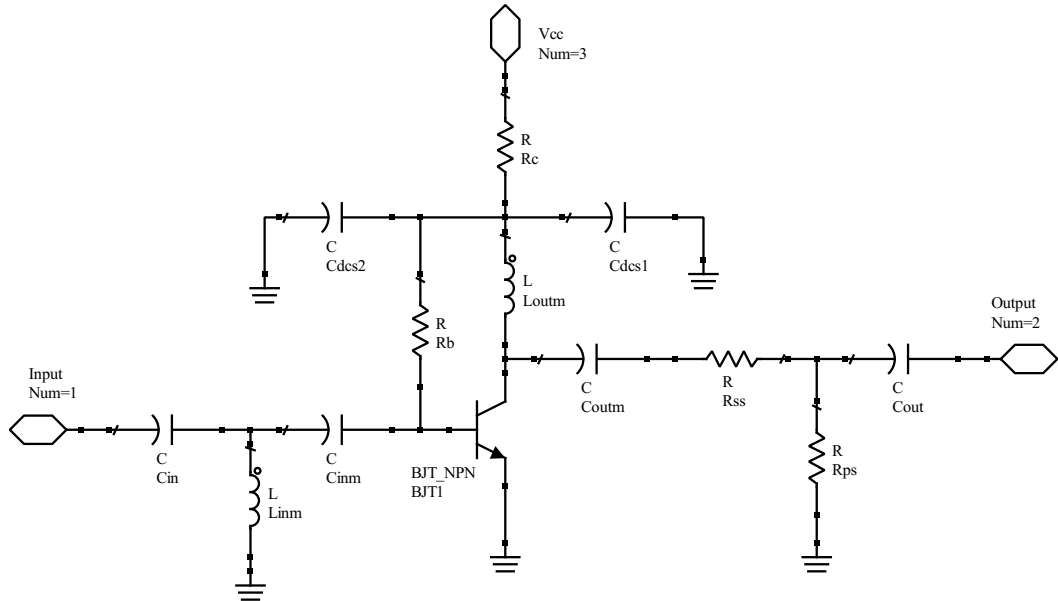


Figure 4.25. Simplified schematic of the 10 dB gain RF amplifier, the component values and its purpose are detailed in Table 4.3.

4.4.2 RF Design Process

The design approach followed in this design is similar to the procedure followed in Section 4.3.3. In the following subsections the stabilization of the transistor, the input and matching network design flow are described.

Stability

The transistor was potentially unstable until 4.25 GHz as shown in Figure 4.15. With the series resistor $R_{ss}=14\ \Omega$ and parallel resistor $R_{ps}=75\ \Omega$ the transistor was made unconditionally stable ($k>1$) in the frequency range from 0 to 10 GHz (Figure 4.26). The schematic used for stabilization is shown in Figure 4.27.

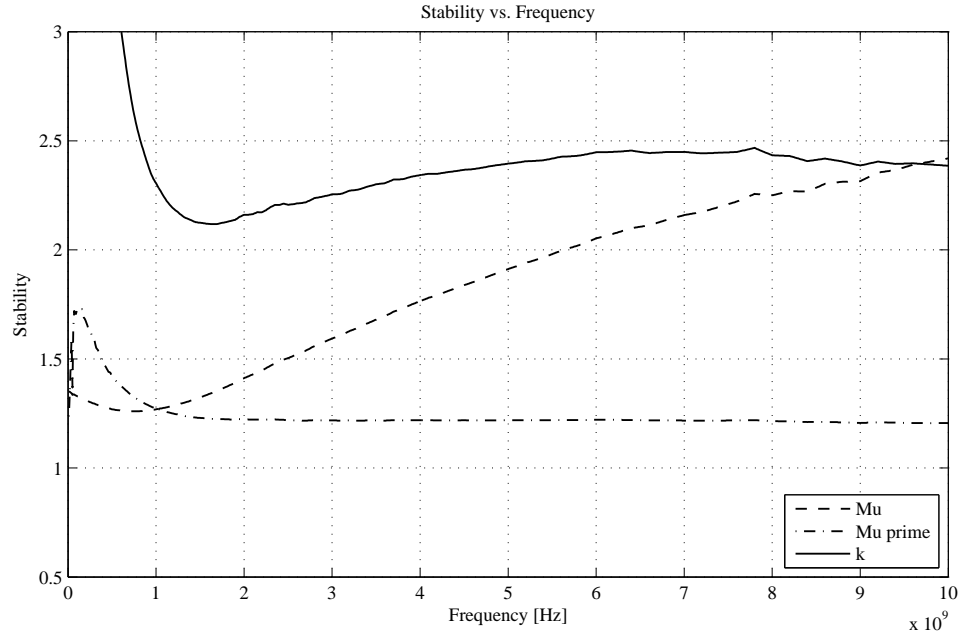


Figure 4.26. Simulated stability factors showing the unconditional stability of the transistor versus frequency.

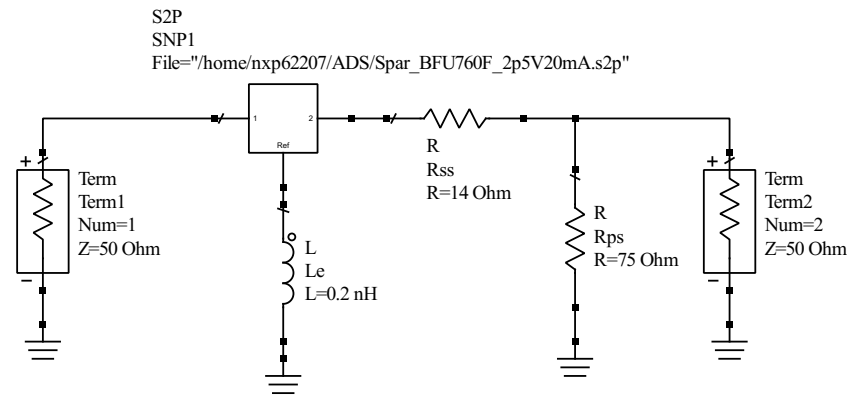


Figure 4.27. Schematic used for the stabilization of the transistor.

Output Matching

The Smith chart describing the load reflection coefficient plane with the constant gain circles at the center frequency of 2.45 GHz is shown in Figure 4.28. The chosen impedance on the 10.5 dB constant circle was $Z_{out}=(40.12+j21.46)\ \Omega$. The

output matching network matched $50\ \Omega$ impedance to Z_{out} with the parallel inductor, $L_{outm}=4.7\ \text{nH}$, and the series capacitor, $C_{outm}=7\ \text{pF}$, at the operating frequency band. The parallel inductor is ground connected through C_{dcs1} . The arrangement of components is shown in Figure 4.25.

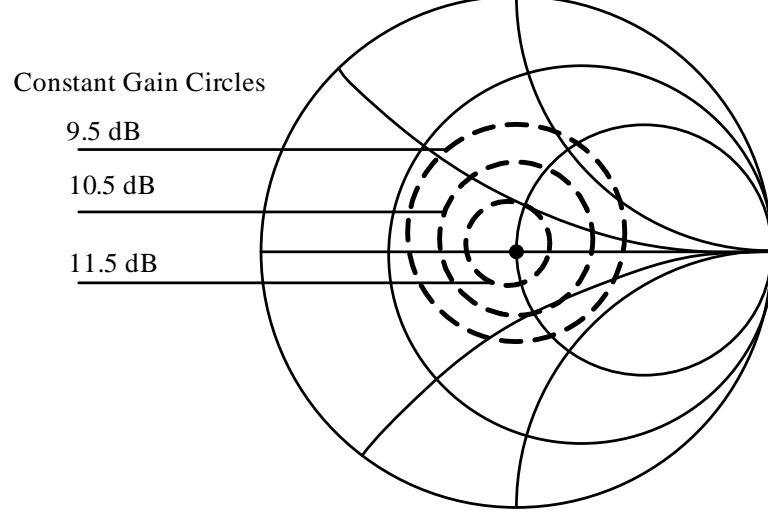


Figure 4.28. Load reflection coefficient with the constant gain circles of the transistor BFU760F at 2.45 GHz frequency with an emitter grounding inductor and stabilization resistors (R_{ss} and R_{ps}).

Input Matching

The input matching network was designed to match the input impedance $Z_{in}=(13.96-j4.73)\ \Omega$ to $50\ \Omega$ source impedance with the parallel inductor $L_{inm}=2.4\ \text{nH}$ and the series capacitor $C_{inm}=1.3\ \text{pF}$ at the operating frequency. The shunt capacitor, C_{dcs2} , and matching components can be noticed in Figure 4.25.

4.4.3 Simulation Results

The final schematic of the amplifier with which simulations were performed within ADS shown in Figure C.1 in Appendix C. The simulated input and output reflection loss of the amplifier are shown in Figure 4.29 from 1 GHz to 4 GHz which covers the operating frequency band. For better visibility the operating frequency band was emphasized with the thick vertical lines at 2.4 GHz and 2.5 GHz.

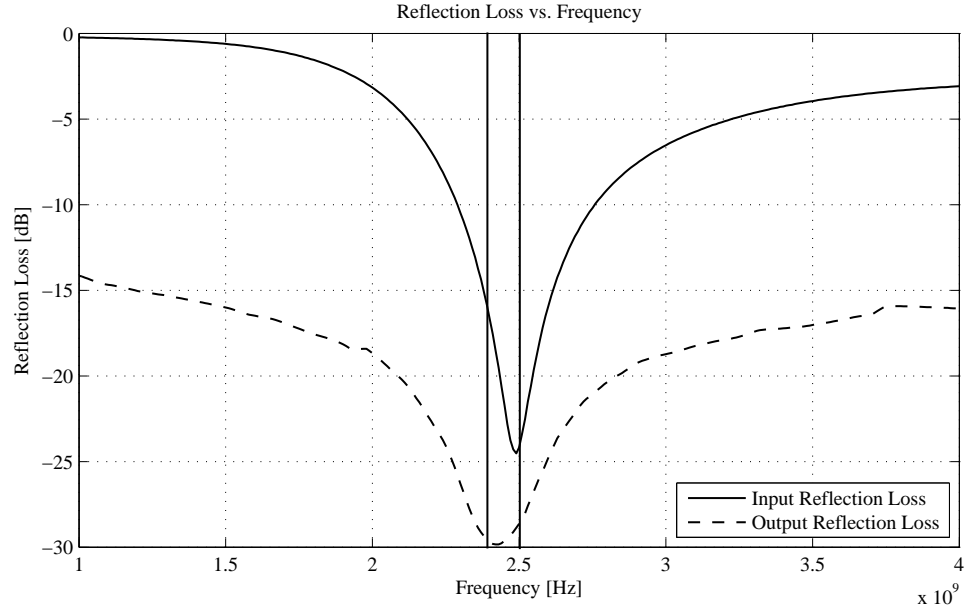


Figure 4.29. Simulated input and output reflection loss of the 10 dB gain amplifier versus frequency.

The simulated gain of the amplifier at 2.4 GHz is 10.25 dB and at 2.5 GHz is 10.15 dB (Figure 4.30). The simulated gain is close to the desired gain. The gain flatness is ± 0.1 dB and is within the design requirement.

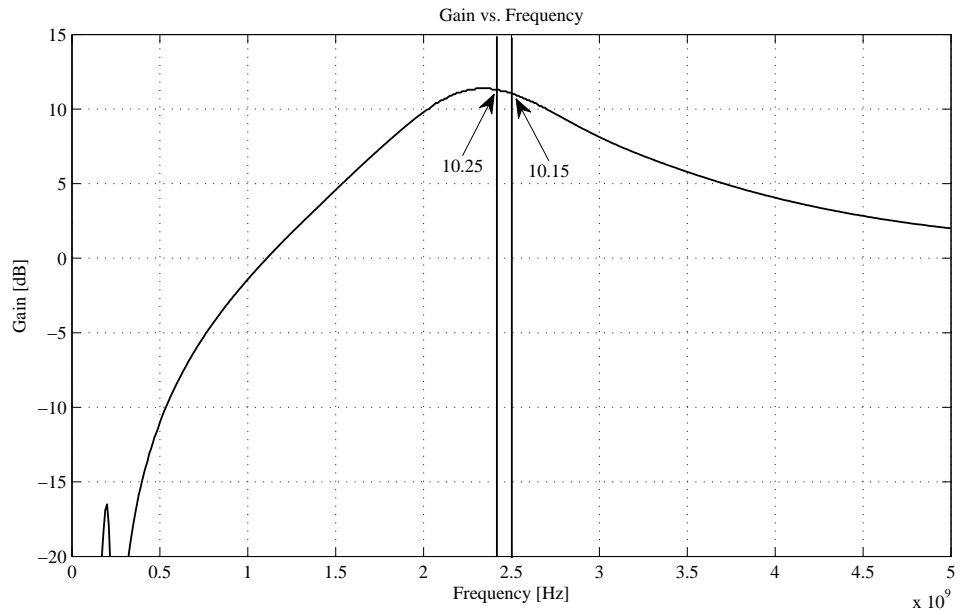


Figure 4.30. Simulated gain of the 10 dB gain amplifier versus frequency.

With the harmonic balance simulations computed OIP3 is 19.3 dBm with spacing of 1 MHz at 2.45 GHz frequency. The output 1-dB gain compression point is 6.5 dBm.

Table 4.3. List of lumped components used for 10 dB gain amplifier.

Component	Simulated	Optimized	Package	Purpose
R_c	40 Ω	24 Ω	0402	DC bias
R_b	40 k Ω	36 k Ω	0402	DC bias
R_{ps}	75 Ω	75 Ω	0402	Stability
R_{ss}	14 Ω	14 Ω	0402	Stability
L_{inm}	2.4 nH	2 nH	0402	Input Matching
L_{outm}	4.7 nH	4.7 nH	0402	Output Matching and DC feed
C_{in}	100 pF	100 pF	0402	DC block
C_{inm}	1.3 pF	1.3 pF	0402	Input Matching
C_{out}	100 pF	100 pF	0402	DC block
C_{outm}	7 pF	10 pF	0402	Output Matching
C_{dcs1}	180 pF	180 pF	0402	High Frequency decoupling
C_{dcs2}	10 nF	10 nF	0402	Decoupling

4.4.4 Layout and Fabrication

The layout was created in ADS is shown in Figure 4.31 (a). It can be observed from the layout that the components are placed freely still the size of the board is 25.87 \times 18.76 mm. With the necessary modifications in the layout of the 17 dB gain amplifier was used in this amplifier. The only change in the layout made was the inclusion of slot for the series stability resistor at the output of the amplifier. A similar procedure as in the 17 dB gain amplifier was followed in milling and fabrication of the amplifier. A photograph of the prototyped amplifier is shown in Figure 4.31 (b).

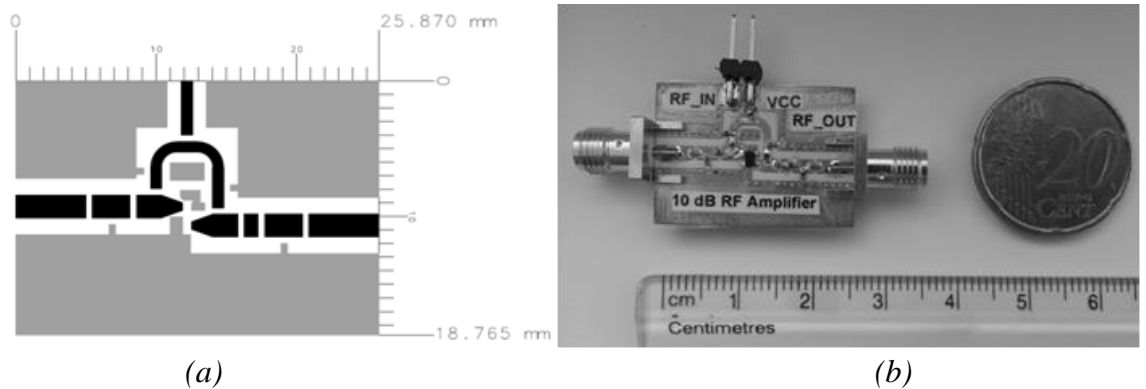


Figure 4.31. 10 dB gain RF amplifier: (a) Layout of the amplifier (Top layer); Gray area: Ground plane, Black area: Signal path (b) Photograph of the prototyped amplifier along with the top of the twenty-euro cent coin and a ruler.

4.4.5 Measurement Results

The measurements were carried out in RF Laboratory in RF Small Signal group at NXP Semiconductors. Both, tuned amplifier measured and actual simulated input and output reflection loss of the amplifier are shown in Figure 4.32. The input and output return loss of the amplifier are 12.5 dB and 30.5 dB respectively at center frequency of 2.45 GHz. The matching network component values were optimized for the best results and the values are presented in Table 4.3. In order to ease the comparison, the measured and simulated gains of the amplifier are shown in same Figure 4.33. It can be observed from the figure that a difference of 1 dB between the measured and simulated results. The measured and simulated stability factor k shows the unconditional stability of the amplifier from 0 to 10 GHz as shown in Figure 4.34. The comparison of design goals, simulations, and measurements results of the 10 dB amplifier are given in Table 4.4.

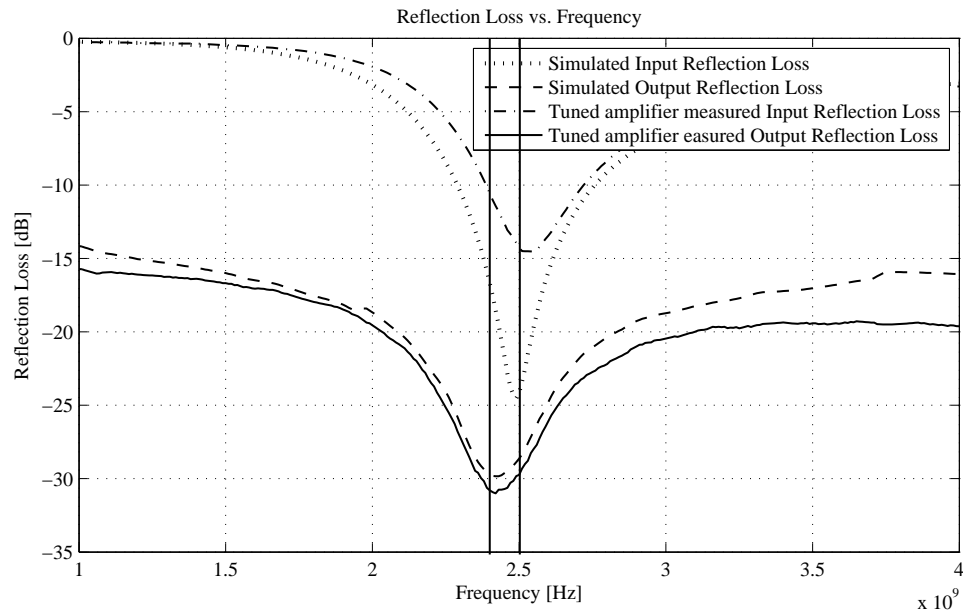


Figure 4.32. Tuned amplifier measured and actual simulated input and output reflection loss of the 10 dB gain amplifier versus frequency.

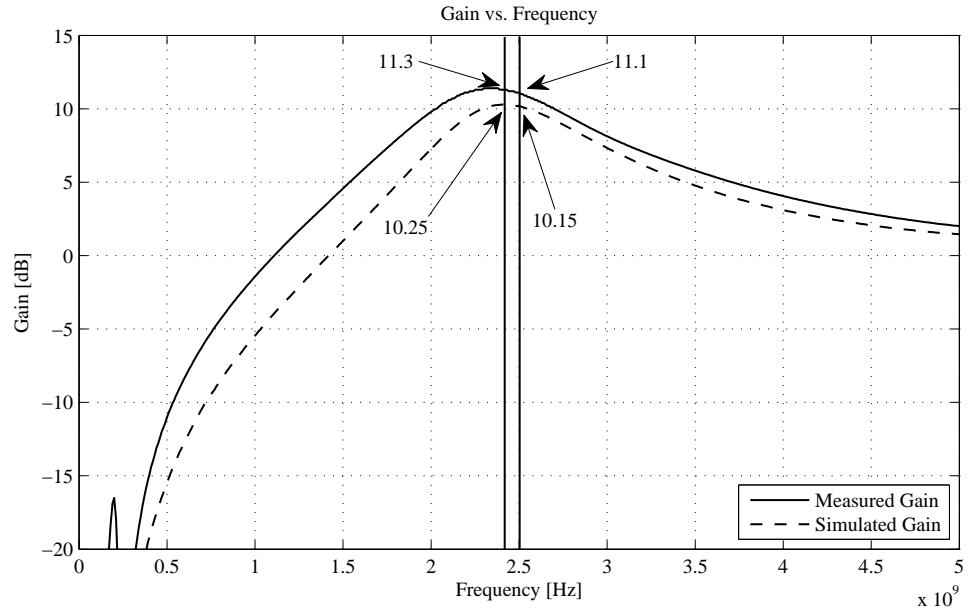


Figure 4.33. Measured and simulated gain of the 10 dB gain amplifier versus frequency.

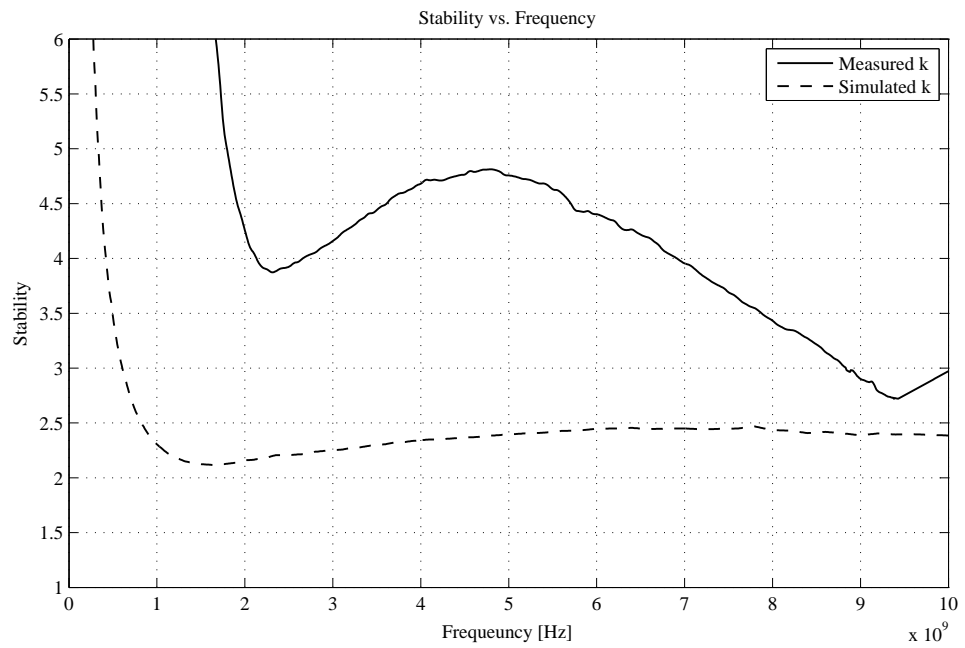


Figure 4.34. Measured and simulated stability factor k of the 10 dB gain amplifier versus frequency.

Table 4.4. Comparison of design goals, simulations, and measurements of 10 dB gain amplifier at 2.45 GHz.

Parameter	Design goals	Simulations	Measurements	Unit	Notes
Supply Voltage	3.3	3.3	3.3	V	
Supply Current	-	20	20	mA	
Center Frequency	2.45	2.45	2.45	GHz	
Bandwidth	100	400	300	MHz	2.4-2.5 GHz
Gain	10	10.1	11.2	dB	
Gain Flatness	± 0.5	± 0.1	± 0.5	dB	
Input Return Loss	10	21.5	12.5	dB	
Output Return Loss	15	29.5	30.5	dB	
Reverse Isolation	-	28.1	28.3	dB	
Output 1-dB Gain Compression Point	6	6.5	5.5	dBm	
OIP3	-	19.3	18	dBm	
Stability					Unconditional Stability
Price	-	-		1.5	€

5. PROTOTYPING

The prototyping of the power divider is described in this chapter. This chapter starts with the design process, which includes the connection of the 3-and 2-way power dividers, 17 dB and 10 dB gain amplifiers together. Next, the simulations and measurements results are presented in Section 5.2 and Section 5.4 respectively. A photograph of the prototyped power divider also presented along with the layout generated in ADS in Section 5.3.

5.1 Design

In the previous chapter (implementation) the 3- and 2-way power dividers, 17 dB and 10 dB gain amplifiers are prototyped as a standalone devices. With this the final design of the power divider can be prototyped with minimum effort and also will take less time in assembling and characterization. Moreover, the trouble shooting becomes much easier. The block diagram showing the interconnection of the dividers and amplifiers are shown in Figure 5.1.

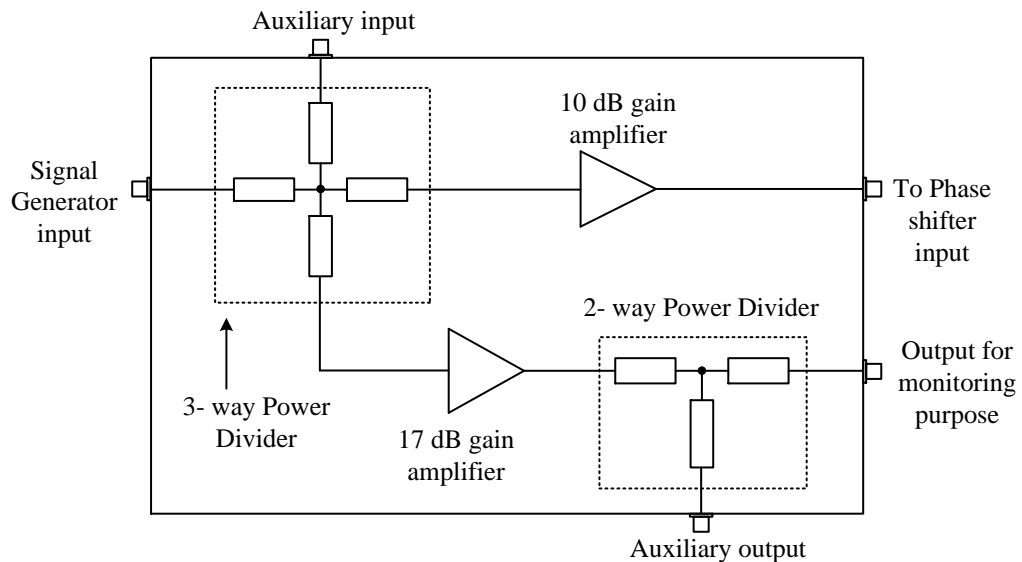


Figure 5.1. Block diagram showing the interconnection of the power dividers and amplifiers.

The topology shown in Figure 5.1 gives the flexibility in configuring the SSB either as a single channel, multi channel master or multi channel slave configuration. In the single channel configuration (Figure 5.2), the auxiliary input and auxiliary output

are terminated with the matched termination i.e. $50\ \Omega$. In this configuration the on-board signal generator (LO) provides the required RF input signal.

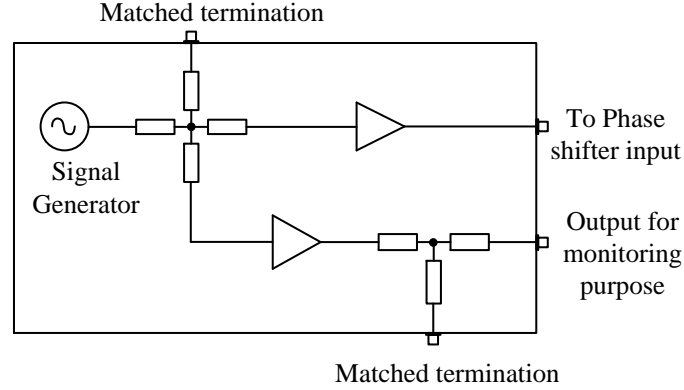


Figure 5.2. Single channel configuration.

In multi channel master configuration, the RF input signal provided by the on-board signal generator and is supplied to the succeeding channels. In the slave configuration, the on-board signal generator is disabled and it gets the RF input signal from the preceding channel. In other words, the second channel receives the RF input signal from the first channel, third channel from the second channel, and so on.

A two channel configuration is shown in Figure 5.3 as an example. The channel 1 is the master which provides the RF input signal to channel 2, which is a slave channel. The signal generator in channel 2 is disabled. The signal generator enabling and disabling is done with the software routine. The auxiliary output of the channel 1 is connected to the auxiliary input of the channel 2. It should be mentioned that, the disabled on-board signal generator acts as a matched termination.

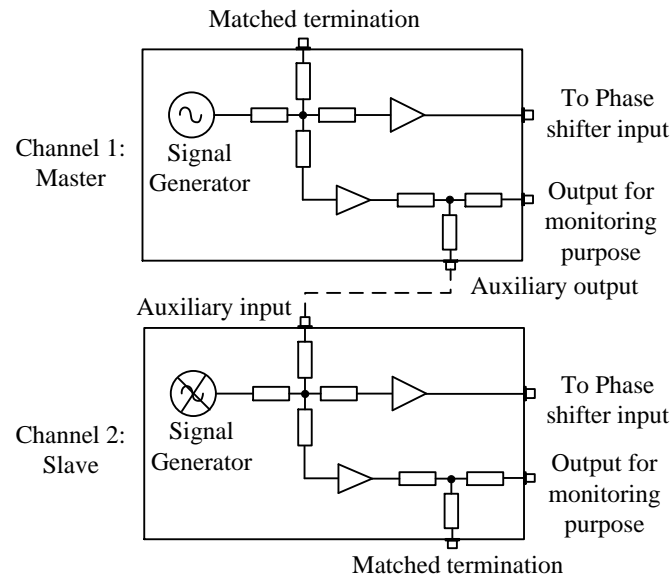


Figure 5.3. Two channel configuration.

5.2 Simulation Results

The schematic that is used for simulations in ADS shown in Figure D.1 in Appendix D. All the schematics which are used previously in developing dividers and amplifiers as standalone devices are connected together through a 50 Ω strip line. Let us label signal generator input as LO in, auxiliary input as Aux in, to phase shifter input as Out 1, output for monitoring purposes as Out 2, and auxiliary output as Aux out (Figure 5.4).

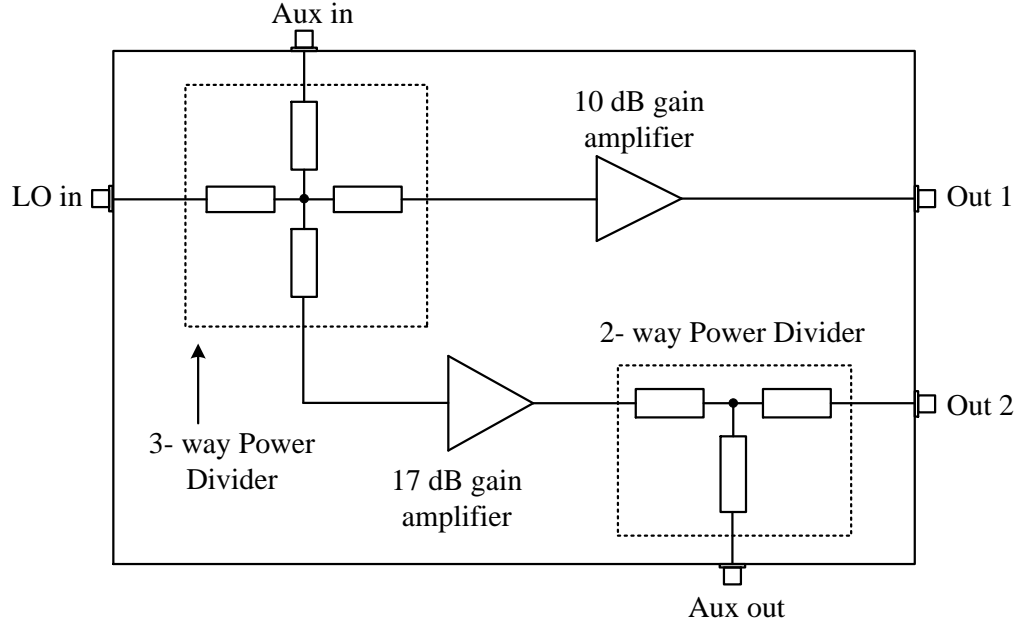


Figure 5.4. Block diagram showing the interconnection of the power dividers and amplifiers and input and output ports are labeled as well.

The gain from the inputs, LO in and Aux in, to the outputs, Out 2 and Aux out, should be 1 dB higher than to Out 1. This is desired to compensate the cable and connector loss of approximately 1 dB (see Section 3.4). The simulated gain between the Aux in and Out 1, Out 2, and Aux out are shown in Figure 5.5 up to 10 GHz frequency. It is clear from the figure that the simulated gain between Aux in and Out 1 is approximately 0 dB and between Aux in and Out 2, Aux out is around 1 dB in the operating frequency band, shown with the dark vertical lines. Similarly, the simulated gain between the LO in and Out 1 is 0.15 dB and between LO in and Out 2, Aux out is 0.92 dB at the center frequency of 2.45 GHz (Figure 5.6). From these results we can conclude that the design has met all the requirements mentioned above.

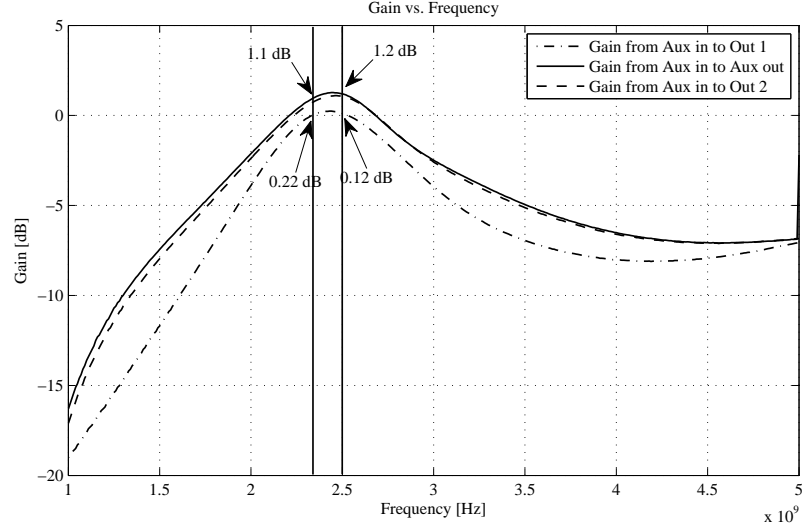


Figure 5.5. Simulated gain between the Aux in and outputs (Out 1, Out 2, and Aux out) versus frequency.

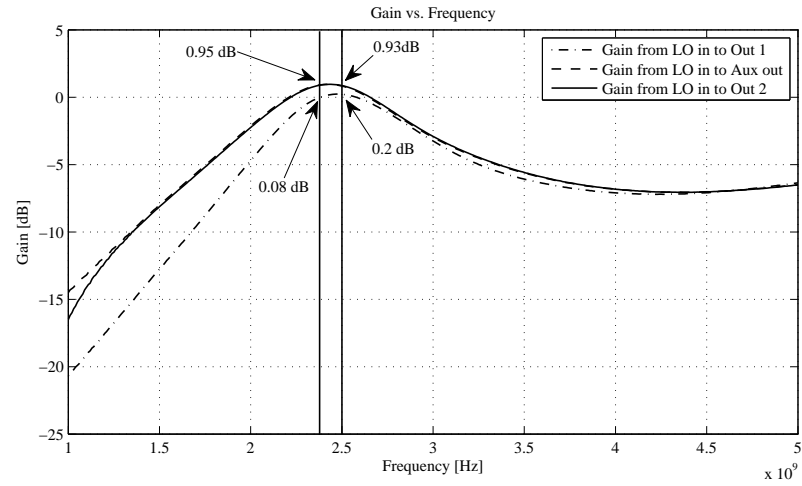


Figure 5.6. Simulated gain between the LO in and outputs (Out 1, Out 2, and Aux out) versus frequency.

5.3 Layout and Fabrication

The layout was created from the schematic in ADS. The amplifiers are configured in such a way that both get the DC bias current from the single DC power supply. It was accomplished by flipping the DC bias path of the 10 dB amplifier to the other side. The difference can be seen in the layout shown in Figure 4.31 (a) and Figure 5.7 (a). The same substrate material that is used for amplifiers was used. Similar procedure like in amplifiers was followed in milling and fabrication. The size of the board is 39.040×34.696 mm. A photograph of the assembled power divider is shown in Figure 5.7 (b). For debugging purposes the DC supply is given to the amplifiers through the $0\ \Omega$ resistors. These resistors are not included in the simulations.

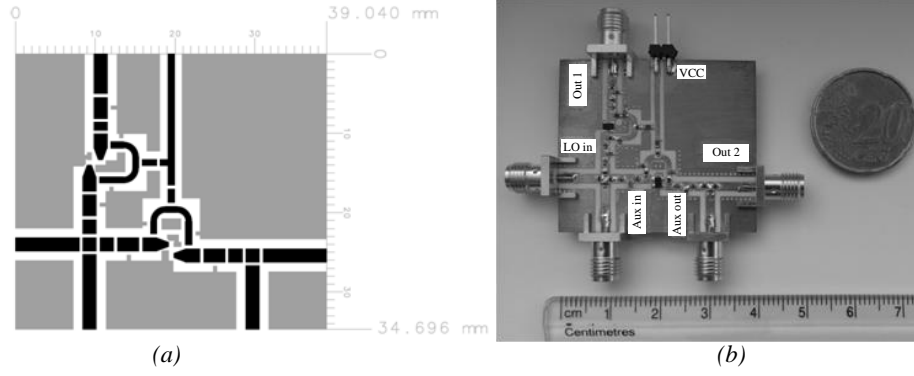


Figure 5.7. Power Divider: (a) Top layer of the layout, (b) Photograph of the prototyped power divider.

5.4 Measurement Results

The measurements are carried out with the assembled power divider as shown in Figure 5.7 (b) in RF Laboratory. The series stability resistor $R_{ss}=14\ \Omega$ in 10 dB gain amplifier is changed to $46\ \Omega$ in order to bring down the gain to the required value. This is the only change made to the assembled power divider. Figure 5.8 shows the measurements results of the gain from Aux in to Out 1, Out 2, and Aux out is 0.35 dB, 1.12 dB, and 0.95 dB respectively at the center frequency of 2.45 GHz. Similarly, the measured gain from LO in to Out 1, Out 2, and Aux out is 0.4 dB, 1.24 dB, and 1.23 dB respectively shown in Figure 5.9. The measured and simulated reflection loss at all input and output ports of the prototyped power divider are shown in Figure 5.10 Table 5.1 shows the comparison of targeted and measurements results at the center frequency of 2.45 GHz.

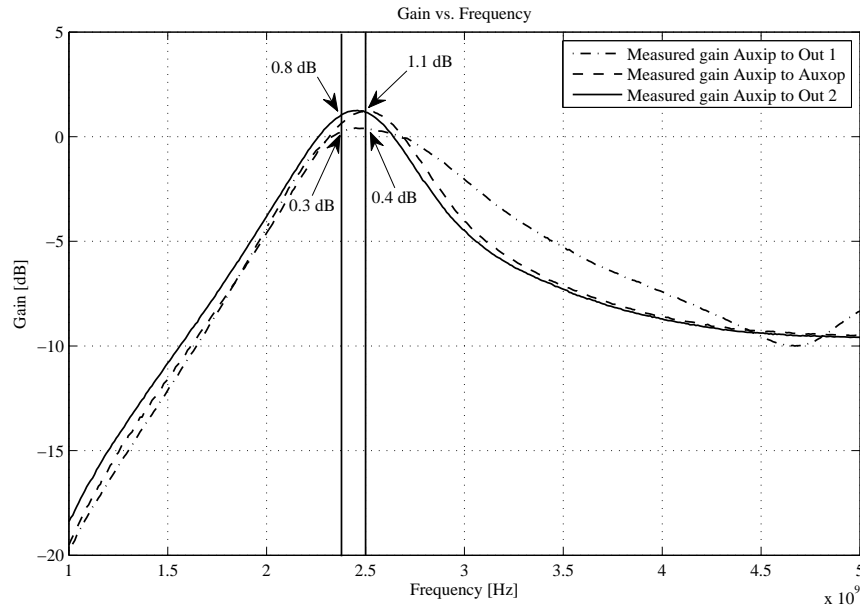


Figure 5.8. Measured gain between the Aux in and outputs (Out 1, Out 2, and Aux out) versus frequency.

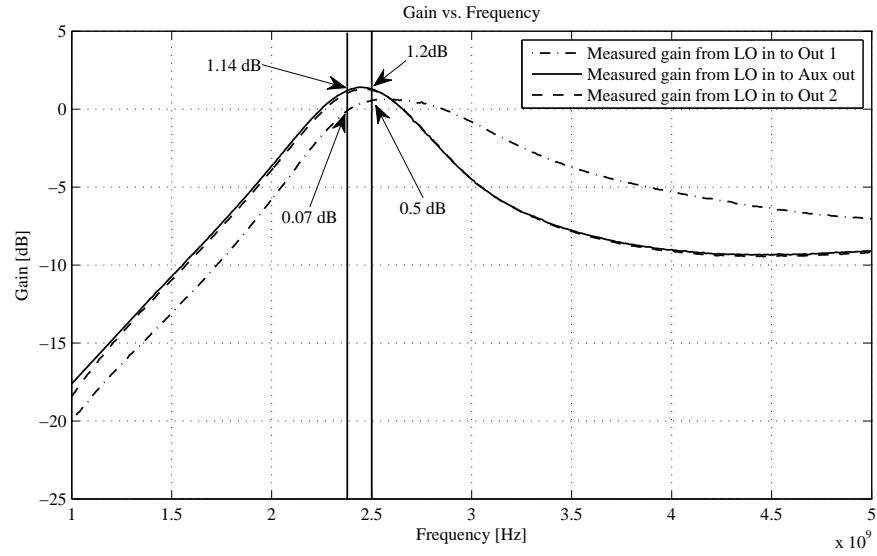


Figure 5.9. Measured gain between the LO in and outputs (Out 1, Out 2, and Aux out) versus frequency.

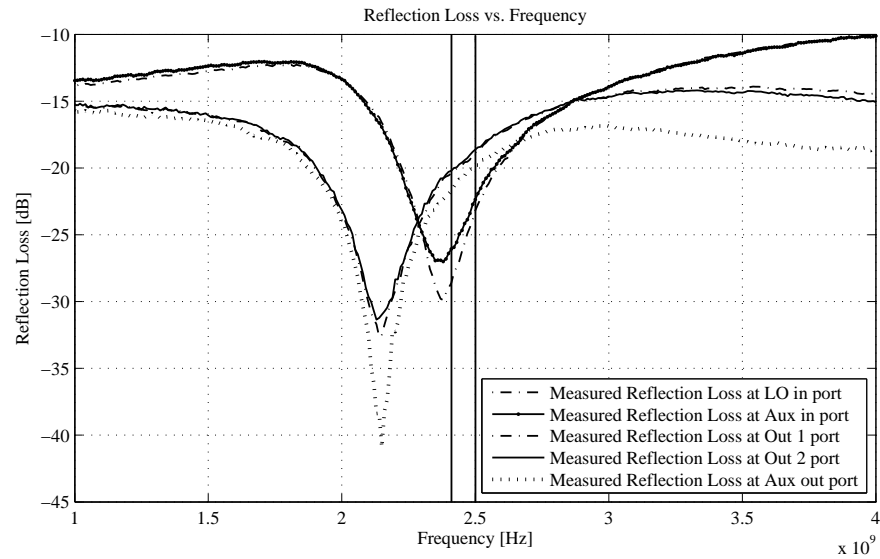


Figure 5.10. Measured and simulated reflection loss of the prototyped 2.4 GHz power divider versus frequency.

Table 5.1. Comparison of targeted and measured gains between the input and output ports.

		Targeted	Simulated	Measured	Unit
Gain from Aux in to	Out 1	0	0.25	0.35	dB
	Out 2	1	1.2	1.12	dB
	Aux out	1	1.22	0.95	dB
Gain from LO in to	Out 1	0	0.21	0.4	dB
	Out 2	1	0.96	1.24	dB
	Aux out	1	0.96	1.23	dB

6. DISCUSSION

This chapter is divided into four sections. In first section, the performance of the prototyped 3-and 2-way resistive power dividers are discussed. The second and third sections covers the performance of the 17 dB and 10 dB gain amplifiers. Finally, in Section 6.4 the performance of the prototyped power divider is presented.

6.1 Power Dividers

6.1.1 3-way Resistive Power Divider

The fabricated 3-way resistive power divider is using $24\ \Omega$, $\pm 5\%$ tolerance, E24 series resistors instead of calculated $25\ \Omega$ resistors. The simulations are carried out with a $24\ \Omega$ ideal resistor. The real $24\ \Omega$ resistor model from the Yageo vendor was not available in ADS library. With the use of $24\ \Omega$ real resistor in prototyping possibility of deviation in the resistor value is about $\pm 1.2\ \Omega$ from the required value. This deviation along with the substrate and practical implementation loss causes the drift in measurement results in comparison to the simulations results. From the Figure 4.5 it can be seen that the deviation in measurements return loss is about 2.2 dB from the simulations results at the center frequency of 2.45 GHz. This is due to the non inclusion of real resistor in simulations and also due to different other factors for example, practical implementation, component tolerances, and substrate loss.. However, the important thing to consider is whether the measured results are within our requirement or not. Similarly, the measured insertion loss is approximately 9.88 dB, 0.38 dB higher than the calculated value of 9.5 dB at 2.45 GHz (see Figure 4.6). The calculated value does not take into account the practical implementation loss. It is important to note that, it is still a prototype, in the final design the calculated value of $25\ \Omega$ with minimum possible tolerance components should be used.

6.1.2 2-way Resistive Power Divider

The prototyped 2-way power divider is using $16\ \Omega$ resistors from the Yageo vendor in the place of calculated $16.6\ \Omega$ resistors. The substrate properties, practical implementation loss, and tolerance of the resistors results in the deviation of measurements results from the simulations results can be noticed in Figure 4.11 and Figure 4.12. The minimum measured return loss is 24 dB and maximum insertion

loss is 6.26 dB in the operating frequency band. It is important to mention that, the actual value of 16.6Ω with a low tolerance value should be used in the final design.

6.2 17 dB Gain Small-Signal RF Amplifier

The 17 dB gain small-signal RF amplifier is prototyped using the bipolar junction transistor BFU760F from the NXP semiconductors. The gain of 17 dB was achieved by designing the output matching network to 17.5 dB constant gain circle plotted on the load reflection coefficient plane of the Smith chart at 2.45 GHz frequency. For compensating the non-idealities of the strip line the matching network is designed for the constant gain circle of 17.5 dB which is 0.5 dB higher than the desired gain. The requirement for the mass production was kept in mind while designing the matching networks. So, the input and output matching networks are designed only with lumped components. The fabricated amplifier was optimized to meet the required goals. The simulations, measurements return loss and gain results are shown in Figure 4.22 and Figure 4.23 respectively. At 2.45 GHz the measured input return loss is 12.5 dB which is 2.5 dB higher than the targeted value and output return loss is 21.5 dB which is 6.5 dB above the desired value. The measured gain is 17.2 dB at 2.45 GHz and is 0.2 dB above the required gain of 17 dB which is not a significant value. Further optimization improves the input and output return loss. As a consequence the gain also increases which is not desired. Therefore, further optimization was not performed. The simulations results predicted the unconditional stability of the amplifier from 0 to 10 GHz, but the measurement results (Figure 4.24) shows potential instability at lower frequencies (less than 100 MHz). This is due to the calibration inaccuracy of the VNA. It was verified that without the power supply to the amplifier the S_{11} was greater than unity. With 20 mA current consumption the achieved output 1-dB gain compression point is 11.4 dBm at 2.45 GHz, which is, however, 0.6 dB less than the targeted value. It is known that highly linear amplifiers normally takes high DC power. High linearity (with respect to OIP3) of 29 dBm was achieved with 66 mW of DC power consumption. The difference in simulations and measurements results is due to the usage of high tolerance lumped components in fabrication instead of tight tolerance components used in the simulations. This is because, unavailability of the tight tolerance components in the fabrication.

Normally, the simulations results do not match with the measured results due to practical differences. From the tuned measurements we can see that, the difference in deviation is not a big value. Still the return loss and gain are good enough for the application. By selecting higher operating currents the output 1-dB gain compression point can be increased but, with the complex matching networks. Furthermore, the higher currents dissipates more heat which should be avoided in our design. By performing electromagnetic co-simulations of the strip line portion of the

circuit the measurements results can be similar to the simulated results. This way, the time required for optimization can be minimized. But, the software which is used for running the electromagnetic co-simulations (momentum) is expensive and it is a time consuming process. So, instead of co-simulation procedure optimization procedure was followed in this design. The price of all components is 1.5 euro shown in Appendix B Table B.2. Except output 1-dB gain compression point the amplifier meets all the design requirements shown in Table 4.2.

6.3 10 dB Gain Small-Signal RF Amplifier

The transistor, BFU760F, that is used for the 17 dB gain amplifier was used for this 10 dB gain amplifier also. Because of the time constraint and other reasons mentioned in Section 4.4.1. From the Figure 4.32 it can be observed that the deviation in the tuned amplifier measured return loss is about 10 dB from the simulated return loss. This is due to the high sensitivity of the input return loss to the component values. A small deviation in component values due to tolerances causes big difference in results. The measured gain is 1.2 dB higher than the targeted gain of 10 dB (Figure 4.33). Further optimization results in decrease of return loss. There is a trade-off between the gain and the input return loss. However, 1.2 dB is not a significant value. The linearity of the amplifier is 18 dBm which is lower linear than 17 dB gain amplifier. Besides DC power the linearity is also function of matching networks. The linearity is also determined with 1-dB gain compression power level. The measured output 1-dB gain compression power level is 5.5 dBm at 2.45 GHz which is close (0.5 dB less) to the required criteria. The bill of material of the amplifier is 1.5 euro (see Appendix C Table C.1). All the design goals (Table 4.4) are met excluding the output 1-dB gain compression power level.

6.4 ISM 2.4 GHz Power Divider with Highly Linear Small-Signal RF Amplifier

The gain and return loss measurements are performed on the prototyped power divider. The deviation from the simulated gain to the measured gain between the inputs and outputs is low. As it can be seen from the Table 5.1 a maximum of 0.28 dB deviation can be noticed between the simulated and measured results of the gain between the LO in and outputs Out 1, Out 2, Aux out which is not a significant value. Similarly, 0.27 dB deviation in gain can be observed between the Aux in and outputs Out 1, Out 2, Aux out. The measured return loss at the input and output ports of the divider are greater than 19 dB at center frequency of 2.45 GHz (Figure 5.10). Except the change of series stability resistor R_{ss} value of 14 Ω to 46 Ω all the other component values are unchanged.

7. CONCLUSION

This thesis report presented the design of a 2.4 GHz ISM band power divider with highly linear small-signal RF amplifier. In order to realize it, 3-and 2-way power dividers, 17 dB and 10 dB gain amplifiers are prototyped as standalone devices and integrated on a single PCB.

The 3-and 2-way resistive power dividers are constructed using resistive power divider topology. The resistive topology has the advantages like, simple to implement, broad band of operation, and compact size. Another major reason for choosing this topology was the requirement for the mass production. It employs only lumped components this makes it easy in mass production with less sensitivity between the constructed dividers. The resistive power dividers are easy to reproduce and are robust. Unless otherwise specified all the presented results are measured at 2.45 GHz in this section. It is recommend to use tight tolerance, 25 Ω and 16.6 Ω resistors in the final design of 3-and 2-way dividers instead of 24 Ω and 16 Ω resistors used in prototyping. The reactive power divider topology can be evaluated as a future work.

Important RF concepts and different amplifier design procedures from different authors are presented and are considered while prototyping the 17 dB and 10 dB small-signal RF amplifiers. The fabricated 17 dB gain amplifier comprises of eleven lumped components and one transistor. The designed and prototyped 17 dB gain amplifier has a gain of 17.2 dB, power consumption of 66 mW, and OIP3 of 29 dBm. Furthermore, the amplifier is unconditionally stable from 0 to 18 GHz. The price of all components is 1.5 euro. The 10 dB gain amplifier was designed such a way that it is possible to re-use the layout of the 17 dB gain amplifier with minor changes in the layout. This way the total time required for designing the layout for the 10 dB gain amplifier was lowered. The only change made in the layout of the 17 dB gain amplifier was the inclusion of extra slot for the series stabilization resistor at the collector of the transistor. The constructed 10 dB amplifier has 11.2 dB gain which is 1.2 dB higher than the desired gain, power consumption of 60 mW, 5.5 dBm of output 1-dB gain compression point, and OIP3 of 18 dBm. The amplifier is unconditionally stable upto 20 GHz. Keeping in mind the requirement of reproducibility with less sensitivity, usage of distributed components for the design of matching networks were avoided in this design. Rogers Corporation's RO4350B LoPro, 30 mil material

used as a substrate. The simple optimization procedure was followed to meet the design goals instead of electromagnetic co-simulations procedure.

A 2.4 GHz ISM band power divider with highly linear small-signal amplifier was realized by integrating all the power dividers and amplifiers on a single substrate. The prototyped power divider has a gain of 0.35 dB between the auxiliary input and Out 1. And, 1.12 dB and 0.95 dB gain between the auxiliary input and Out 2, auxiliary output. Furthermore, the gain between the LO input and Out 1 is 0.4 dB. And, 1.24 dB and 1.23 dB between LO input and Out 2, auxiliary output. By fabricating each device as a standalone device the final prototype was built with minimum effort and in less time. Furthermore, the cost of the power divider is 3.5 euro. The prototyped power divider is ready to be used for the needs of the small-signal board that is used in the solid state cooking project.

It is interesting to perform electromagnetic co-simulations of the strip line portion of the circuit as a future work. Furthermore, the 10 dB amplifier can be designed and constructed with different DC bias current as a further work and also with different transistor. Minimum tolerance lumped components from the other vendor can be evaluated as a further work. The Monte Carlo analysis should be performed for the analysis of the volume manufacturability by including variability of the PCB material and lumped components tolerances. The power divider can be evaluated for other ISM frequency bands.

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A. APPENDIX: DETAILED DATA OF PROTOTYPED RESISTIVE POWER DIVIDERS

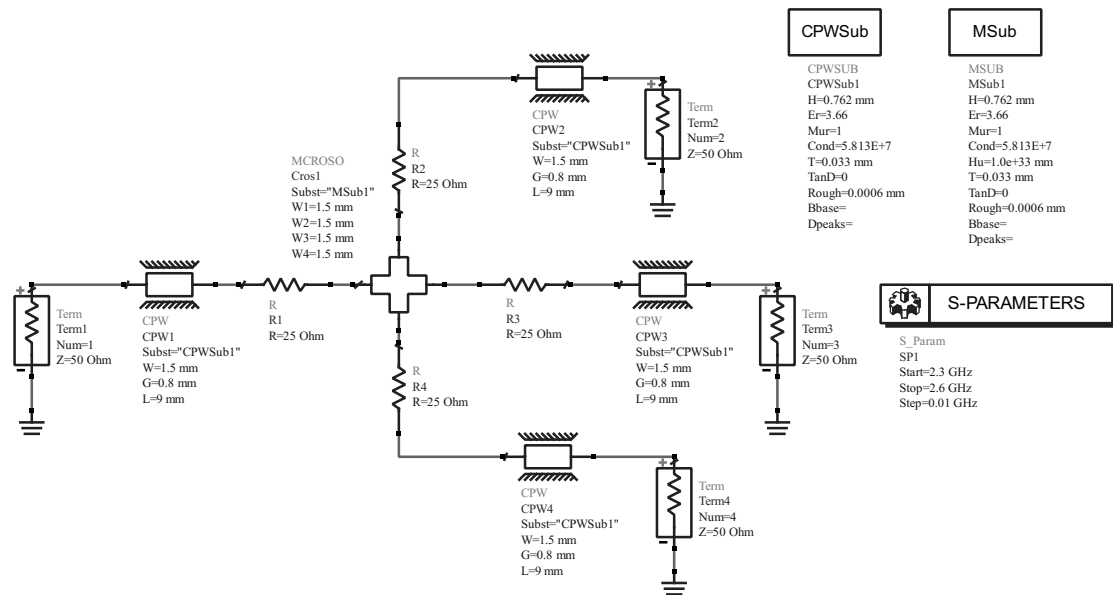
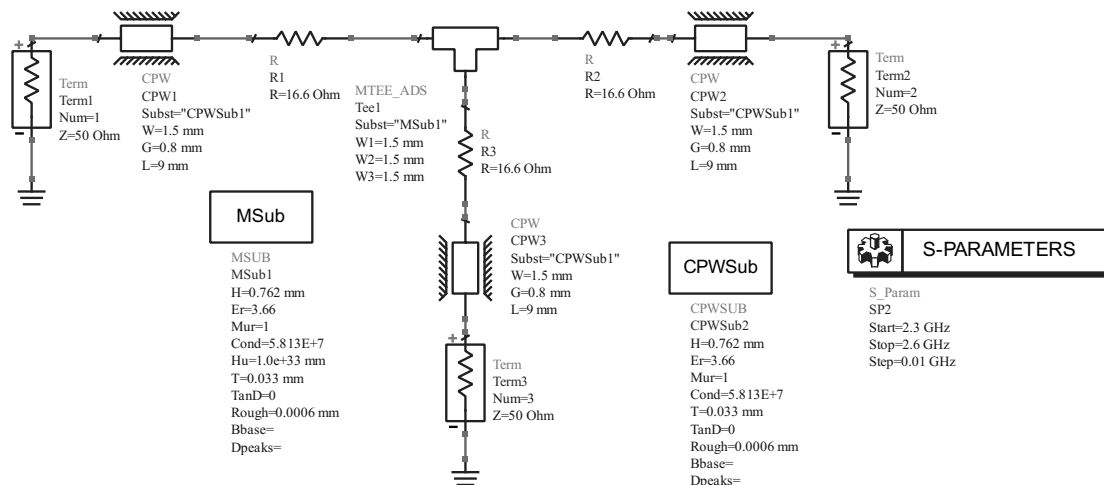


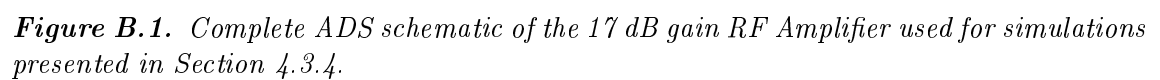
Figure A.1. 3-way resistive power divider simulations schematic with the ideal $24\ \Omega$ resistors at four ports along with the strip lines.



B. APPENDIX: DETAILED DATA OF PROTOTYPED 17 DB GAIN RF AMPLIFIER

Table B.1. *S*-parameters of the transistor BFU760F for DC bias $V_{CE}=2.5$ V and $I_C=20$ mA.

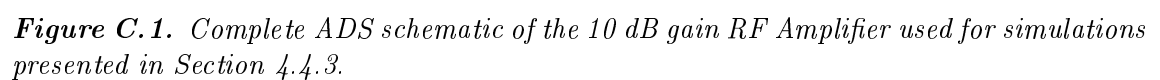
Freq-	S11-	S11-	S21-	S21-	S12-	S12-	S22-	S22-
MHz	mag	arg	mag	arg	mag	arg	mag	arg
2400	0.678	179	8.02	75.07	0.05	36.27	0.273	-152.3
2450	0.678	178	7.86	74.47	0.05	36.43	0.272	-153.3
2500	0.679	177	7.7	73.86	0.051	36.54	0.271	-154.5



Please note that the prices of the components are in the order of minimum number of fifty components. The prices are from Mouser electronics [38] on the date 7 July, 2013.

Table B.2. *Bill of Material of 17 dB gain RF amplifier.*

Component	Package	Price in €
BJT	SOT343F	0.273
R_c	0402	0.0001
R_b	0402	0.0001
R_{ps}	0402	0.0001
L_{inm}	0402	0.1
L_{outm}	0402	0.218
C_{in}	0402	0.018
C_{inm}	0402	0.018
C_{out}	0402	0.018
C_{outm}	0402	0.018
C_{dcs1}	0402	0.018
C_{dcs2}	0402	0.018
PCB	-	0.5



Please note that the prices of the components are in the order of minimum number of fifty components. The prices are from Mouser electronics [38] on the date 7 July, 2013.

Table C.1. *Bill of Material of 10 dB gain RF amplifier.*

Component	Package	Price in €
BJT	SOT343F	0.273
R_c	0402	0.0001
R_b	0402	0.0001
R_{ps}	0402	0.0001
R_{ss}	0402	0.0001
L_{inm}	0402	0.1
L_{outm}	0402	0.218
C_{in}	0402	0.018
C_{inm}	0402	0.018
C_{out}	0402	0.018
C_{outm}	0402	0.018
C_{dcs1}	0402	0.018
C_{dcs2}	0402	0.018
PCB	-	0.5

D. APPENDIX: DETAILED DATA OF 2.4 GHZ POWER DIVIDER WITH HIGHLY LINEAR SMALL-SIGNAL RF AMPLIFIER

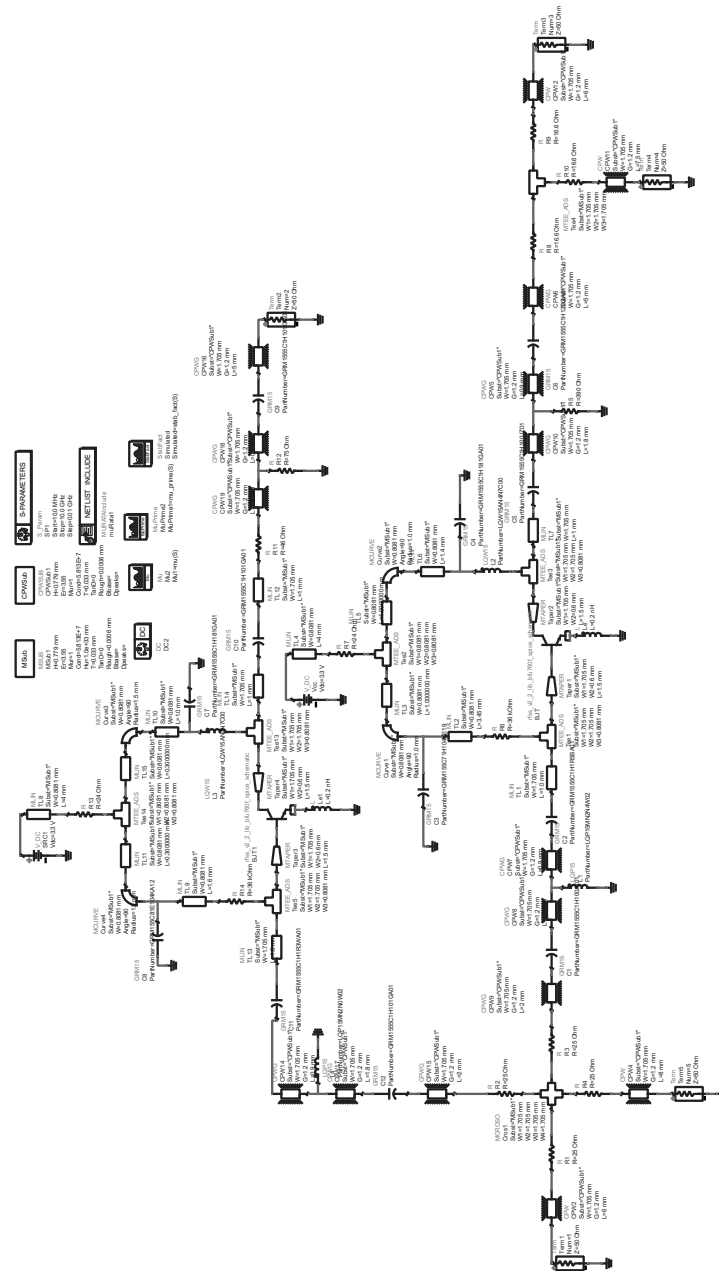


Figure D.1. ADS schematic of the complete integration of the power dividers and amplifiers used for simulations presented in Section 5.2.